SRC4190(1)



SBFS023A – JUNE – REVISED JULY 2003

192kHz Stereo Asynchronous Sample Rate Converters

FEATURES

- **AUTOMATIC SENSING OF THE INPUT-TO-OUTPUT SAMPLING RATIO**
- **WIDE INPUT-TO-OUTPUT SAMPLING RANGE: 16:1 to 1:16**
- **SUPPORTS INPUT AND OUTPUT SAMPLING RATES UP TO 212kHz**
- **DYNAMIC RANGE: 128dB (–60dbFS input, BW = 20Hz to $f_S/2$, A-Weighted)**
- **THD+N: –125dB (0dbFS input, BW = 20Hz to $f_S/2$)**
- **ATTENUATES SAMPLING AND REFERENCE CLOCK JITTER**
- **HIGH PERFORMANCE, LINEAR PHASE DIGITAL FILTERING**
- **FLEXIBLE AUDIO SERIAL PORTS:**
  - **Master or Slave Mode Operation**
  - **Supports I^2S, Left Justified, Right Justified, and TDM Data Formats**
  - **Supports 16, 18, 20, or 24-Bit Audio Data**
  - **TDM Mode allows daisy chaining of up to eight devices**
- **SUPPORTS 24-, 20-, 18-, or 16-BIT INPUT AND OUTPUT DATA**
  - **All output data is dithered from the internal 28-Bit data path**
- **LOW GROUP DELAY OPTION FOR INTERPOLATION FILTER**
- **SOFT MUTE FUNCTION**
- **BYPASS MODE**
- **POWER DOWN MODE**
- **OPERATES FROM A SINGLE +3.3 VOLT POWER SUPPLY**
- **SMALL SSOP-28 PACKAGE**
- **PIN COMPATIBLE WITH THE SRC4192, AD1895, AND AD1896(2)**

APPLICATIONS

- **DIGITAL MIXING CONSOLES**
- **DIGITAL AUDIO WORKSTATIONS**
- **AUDIO DISTRIBUTION SYSTEMS**
- **BROADCAST STUDIO EQUIPMENT**
- **HIGH-END A/V RECEIVERS**
- **GENERAL DIGITAL AUDIO PROCESSING**

DESCRIPTION

The SRC4190 is an asynchronous sample rate converter designed for professional and broadcast audio applications. The SRC4190 combines a wide input-to-output sampling ratio with outstanding dynamic range and low distortion. Input and output serial ports support standard audio formats, as well as a Time Division Multiplexed (TDM) mode. Flexible audio interfaces allow the SRC4190 to connect to a wide range of audio data converters, digital audio receivers and transmitters, and digital signal processors.

The SRC4190 is a standalone pin-programmed device, with control pins for mode, data format, mute, bypass, and low group delay functions.

The SRC4190 may be operated from a single +3.3V power supply. A separate digital I/O supply (V_{IO}) operates over the +1.65V to +3.6V supply range, allowing greater flexibility when interfacing to current and future generation signal processors and logic devices. The SRC4190 is available in a SSOP-28 package.

(1) Patents Pending.
(2) Refer to the Applications Information section of this data sheet for details.

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ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage, V_{DD}	–0.3V to +4.0V
Supply Voltage, V_{IO}	–0.3V to +4.0V
Digital Input Voltage	–0.3V to +4.0V
Operating Temperature Range	–45°C to +85°C
Storage Temperature Range	–65°C to +150°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

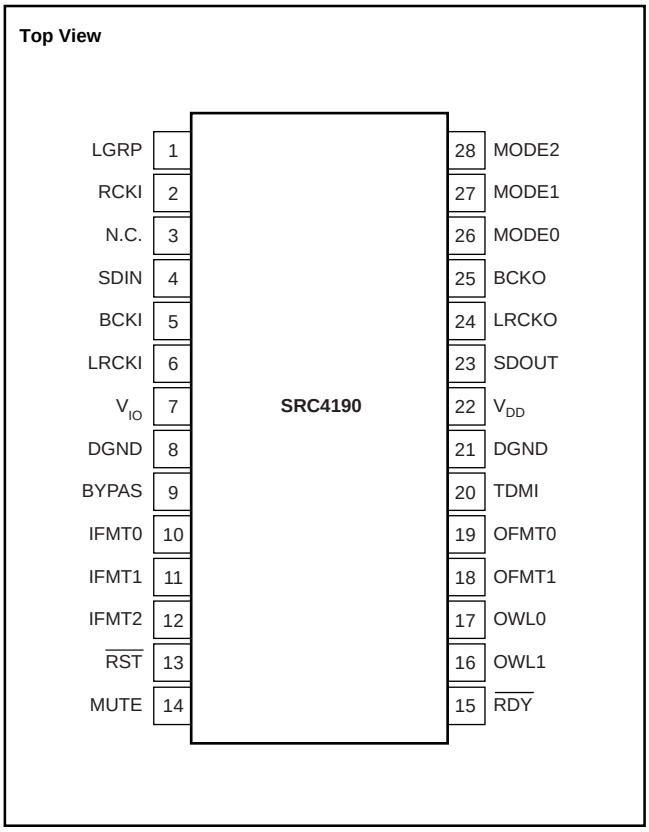
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
SRC4190	SSOP-28	DB	–45°C to +85°C	SRC4190I	SRC4190IDB	Rails, 50
"	"	"	"	"	SRC4190IDBR	Tape and Reel, 2000

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

PIN CONFIGURATION (SRC4190)

Top View



PIN DESCRIPTIONS (SRC4190)

PIN#	NAME	DESCRIPTION
1	LGRP	Low Group Delay Control Input (Active High)
2	RCKI	Reference Clock Input
3	N.C.	No Connection
4	SDIN	Audio Serial Data Input
5	BCKI	Input Port Bit Clock I/O
6	LRCKI	Input Port Left/Right Word Clock I/O
7	V_{IO}	Digital I/O Supply, +1.65V to V_{DD}
8	DGND	Digital Ground
9	BYPAS	ASRC Bypass Control Input (Active High)
10	IFMT0	Input Port Data Format Control Input
11	IFMT1	Input Port Data Format Control Input
12	IFMT2	Input Port Data Format Control Input
13	$\overline{RST}$	Reset Input (Active Low)
14	MUTE	Output Mute Control Input (Active High)
15	$\overline{RDY}$	ASRC Ready Status Output (Active Low)
16	OWL1	Output Port Data Word Length Control Input
17	OWL0	Output Port Data Word Length Control Input
18	OFMT1	Output Port Data Format Control Input
19	OFMT0	Output Port Data Format Control Input
20	TDMI	TDM Data Input (Connect to DGND when not in use)
21	DGND	Digital Ground
22	V_{DD}	Digital Core Supply, +3.3V
23	SDOUT	Audio Serial Data Output
24	LRCKO	Output Port Left/Right Word Clock I/O
25	BCKO	Output Port Bit Clock I/O
26	MODE0	Serial Port Mode Control Input
27	MODE1	Serial Port Mode Control Input
28	MODE2	Serial Port Mode Control Input

ELECTRICAL CHARACTERISTICS

All parameters specified with T_A = +25°C, V_{DD} = +3.3V, and V_{IO} = +3.3V, unless otherwise noted.

PARAMETER		CONDITION	SRC4190 MIN	SRC4190 TYP	SRC4190 MAX	UNITS
DYNAMIC PERFORMANCE(1)						
Resolution				24		Bits
Input Sampling Frequency	f_{SIN}		4		212	kHz
Output Sampling Frequency	f_{SOUT}		4		212	kHz
Input: Output Sampling Ratio						
Upsampling					1:16	
Downsampling					16:1	
Dynamic Range		BW = 20Hz to f_{SOUT}/2, –60dBFS Input f_{IN} = 1kHz, Unweighted (add 3dB to spec for A-weighted result)				
44.1kHz:48kHz				125		dB
48kHz:44.1kHz				125		dB
48kHz:96kHz				125		dB
44.1kHz:192kHz				125		dB
96kHz:48kHz				125		dB
192kHz:12kHz				125		dB
192kHz:32kHz				125		dB
192kHz:48kHz				125		dB
32kHz:48kHz				125		dB
12kHz:192kHz				125		dB
Total Harmonic Distortion + Noise		BW = 20Hz to f_{SOUT}/2, 0dBFS Input f_{IN} = 1kHz, Unweighted				
44.1kHz:48kHz				–125		dB
48kHz:44.1kHz				–125		dB
48kHz:96kHz				–125		dB
44.1kHz:192kHz				–125		dB
96kHz:48kHz				–125		dB
192kHz:12kHz				–125		dB
192kHz:32kHz				–125		dB
192kHz:48kHz				–125		dB
32kHz:48kHz				–125		dB
12kHz:192kHz				–125		dB
Interchannel Gain Mismatch				0		dB
Interchannel Phase Deviation				0		Degrees
Mute Attenuation		24-Bit Word Length, A-weighted		–128		dB
DIGITAL INTERPOLATION FILTER CHARACTERISTICS						
Passband					0.4535 x f_{SIN}	Hz
Passband Ripple					±0.007	dB
Transition Band			0.4535 x f_{SIN}		0.5465 x f_{SIN}	Hz
Stop Band			0.5465 x f_{SIN}			Hz
Stop Band Attenuation			–125			dB
Normal Group Delay (LGRP = 0)				102.53125/f_{SIN}		Seconds
Low Group Delay (LGRP = 1)				70.53125/f_{SIN}		Seconds
DIGITAL DECIMATION FILTER CHARACTERISTICS						
Passband					0.4535 x f_{SOUT}	Hz
Passband Ripple					±0.008	dB
Transition Band			0.4535 x f_{SOUT}		0.5465 x f_{SOUT}	Hz
Stop Band			0.5465 x f_{SOUT}			Hz
Stop Band Attenuation			–125			dB
Group Delay				36.46875/f_{SOUT}		Seconds
DIGITAL I/O CHARACTERISTICS						
High-Level Input Voltage	V_{IH}		0.7 x V_{IO}		V_{IO}	V
Low Level Input Voltage	V_{IL}		0		0.3 x V_{IO}	V
High-Level Input Current	I_{IH}			0.5	10	µA
Low-Level Input Current	I_{IL}			0.5	10	µA
High-Level Output Voltage	V_{OH}	I_O = –4mA	0.8 x V_{IO}		V_{IO}	V
Low-Level Output Voltage	V_{OL}	I_O = +4mA	0		0.2 x V_{IO}	V
Input Capacitance	C_{IN}			3		pF

NOTES: (1) Dynamic performance measured with an Audio Precision System Two Cascade or Cascade Plus.
(2) f_{SMIN} = min (f_{SIN}, f_{SOUT}).
(3) f_{SMAX} = max (f_{SIN}, f_{SOUT}).

ELECTRICAL CHARACTERISTICS (Cont.)

All parameters specified with T_A = +25°C, V_{DD} = +3.3V, and V_{IO} = +3.3V, unless otherwise noted.

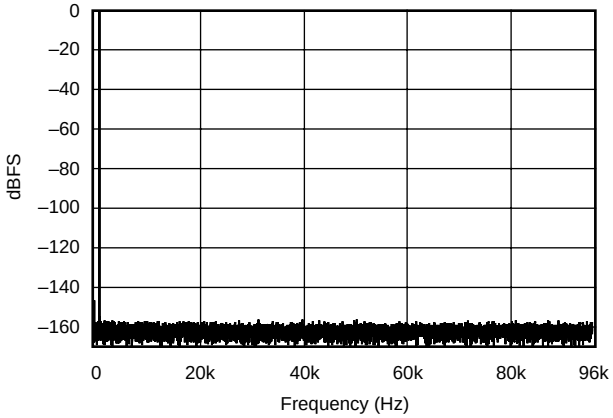
PARAMETER		CONDITION	SRC4190 MIN	SRC4190 TYP	SRC4190 MAX	UNITS
SWITCHING CHARACTERISTICS						
Reference Clock Timing						
RCKI Frequency[2, 3]			128 x f_{SMIN}		50	MHz
RCKI Period	t_{RCKIP}		20		1/(128 x f_{SMIN})	ns
RCKI Pulsewidth High	t_{RCKIH}		0.4 x t_{RCKIP}			ns
RCKI Pulsewidth Low	t_{RCKIL}		0.4 x t_{RCKIP}			ns
Reset Timing						
$\overline{RST}$ Pulse Width Low	t_{RSTL}		500			ns
Input Serial Port Timing						
LRCKI to BCKI Setup Time	t_{LRIS}		10			ns
BCKI Pulsewidth High	t_{SIH}		10			ns
BCKI Pulsewidth Low	t_{SIL}		10			ns
SDIN Data Setup Time	t_{LDIS}		10			ns
SDIN Data Hold Time	t_{LDIH}		10			ns
Output Serial Port Timing						
SDOUT Data Delay Time	t_{DOPD}				10	ns
SDOUT Data Hold Time	t_{DOH}		2			ns
BCKO Pulsewidth High	t_{SOH}		10			ns
BCKO Pulsewidth Low	t_{SOL}		5			ns
TDM Mode Timing						
LRCKO Setup Time	t_{LROS}		10			ns
LRCKO Hold Time	t_{LROH}		10			ns
TDMI Data Setup Time	t_{TDMS}		10			ns
TDMI Data Hold Time	t_{TDMH}		10			ns
POWER SUPPLIES						
Operating Voltage						
V_{DD}			3.0	+3.3	3.6	V
V_{IO}			1.65	+3.3	3.6	V
Supply Current		V_{DD} = +3.3V, V_{IO} = +3.3V				
I_{DD}, Power Down		$\overline{RST}$ = 0, No Clocks			100	µA
I_{DD}, Dynamic		f_{SIN} = f_{SOUT} = 192kHz		66		mA
I_{IO}, Power Down		$\overline{RST}$ = 0, No Clocks			100	µA
I_{IO}, Dynamic		f_{SIN} = f_{SOUT} = 192kHz		2		mA
Total Power Dissipation		V_{DD} = +3.3V, V_{IO} = +3.3V				
P_D, Power Down		$\overline{RST}$ = 0, No Clocks			660	µW
P_D, Dynamic		f_{SIN} = f_{SOUT} = 192kHz		225		mW

NOTES: (1) Dynamic performance measured with an Audio Precision System Two Cascade or Cascade Plus.
(2) f_{SMIN} = min (f_{SIN}, f_{SOUT}).
(3) f_{SMAX} = max (f_{SIN}, f_{SOUT}).

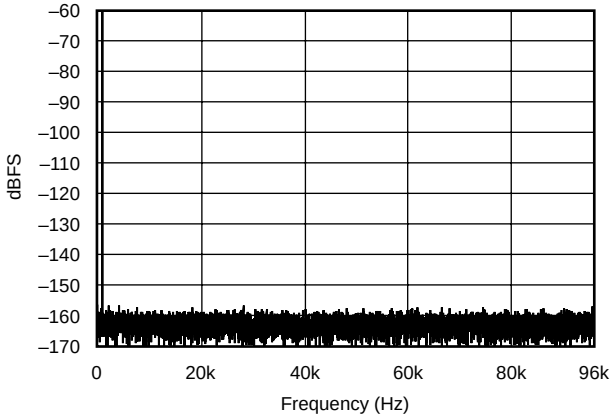
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_{DD} = +3.3V, and V_{IO} = +3.3V, unless otherwise noted.

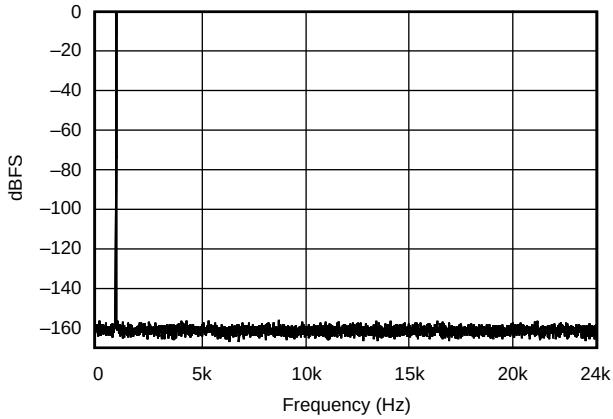
FFT with 1kHz INPUT TONE at 0dBFS
(12kHz:192kHz)



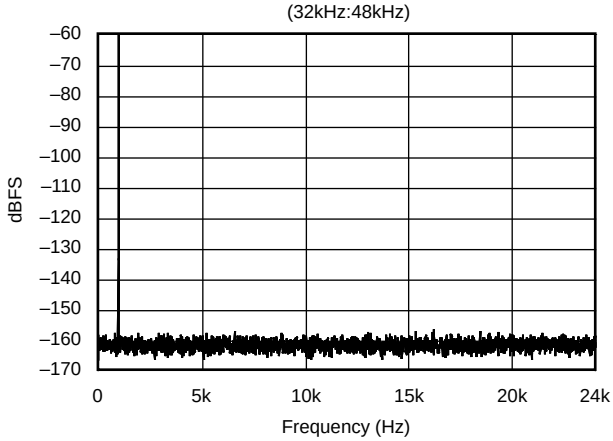
FFT with 1kHz INPUT TONE at –60dBFS
(12kHz:192kHz)



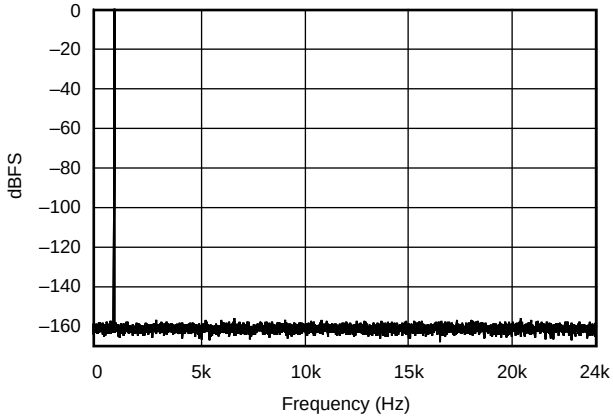
FFT with 1kHz INPUT TONE at 0dBFS
(32kHz:48kHz)



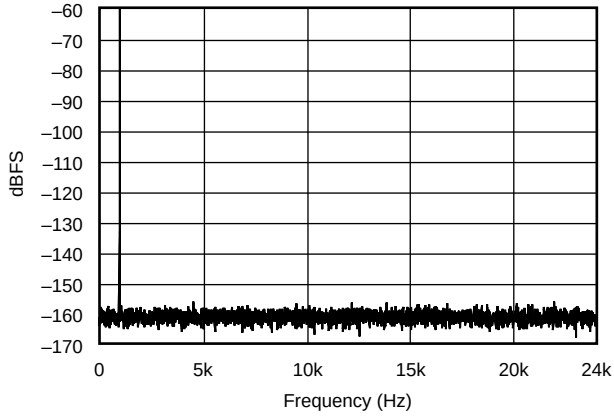
FFT with 1kHz INPUT TONE at –60dBFS
(32kHz:48kHz)



FFT with 1kHz INPUT TONE at 0dBFS
(44.1kHz:48kHz)



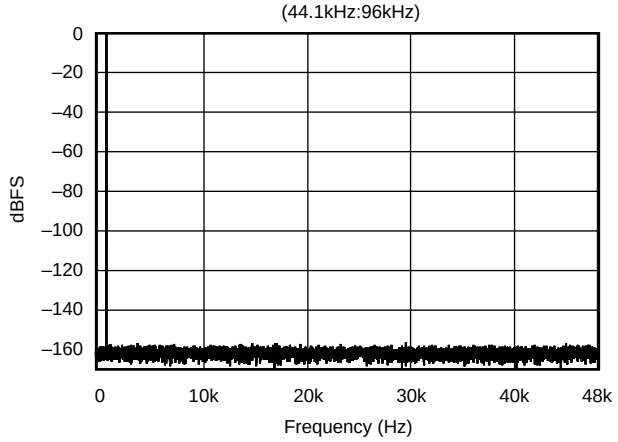
FFT with 1kHz INPUT TONE at –60dBFS
(44.1kHz:48kHz)



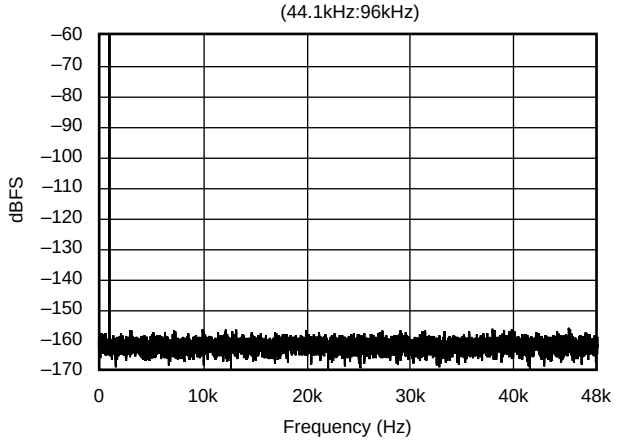
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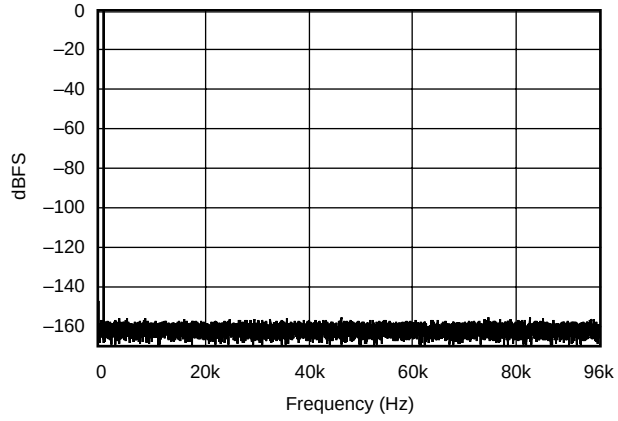
FFT with 1kHz INPUT TONE at 0dBFS
(44.1kHz:96kHz)



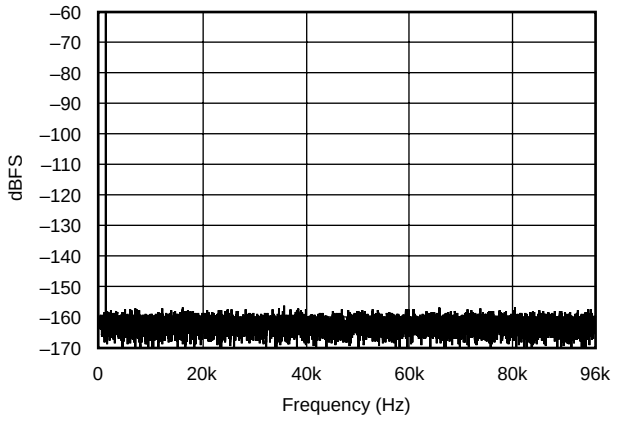
FFT with 1kHz INPUT TONE at –60dBFS
(44.1kHz:96kHz)



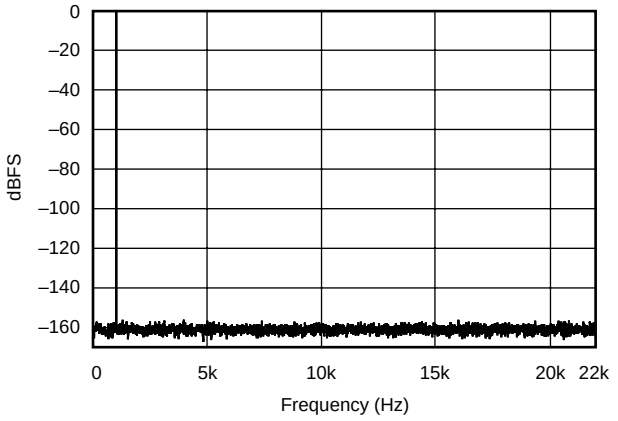
FFT with 1kHz INPUT TONE at 0dBFS
(44.1kHz:192kHz)



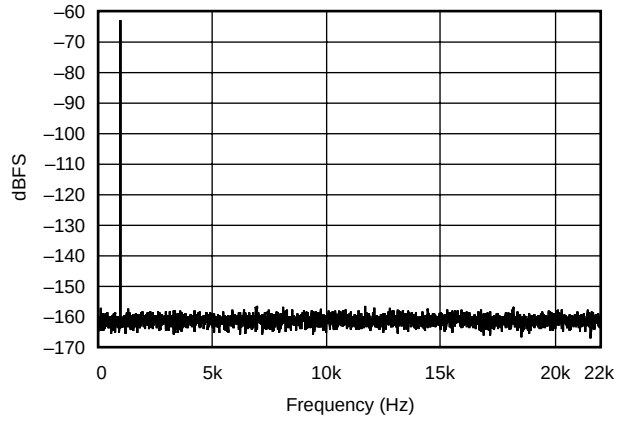
FFT with 1kHz INPUT TONE at –60dBFS
(44.1kHz:192kHz)



FFT with 1kHz INPUT TONE at 0dBFS
(48kHz:44.1kHz)



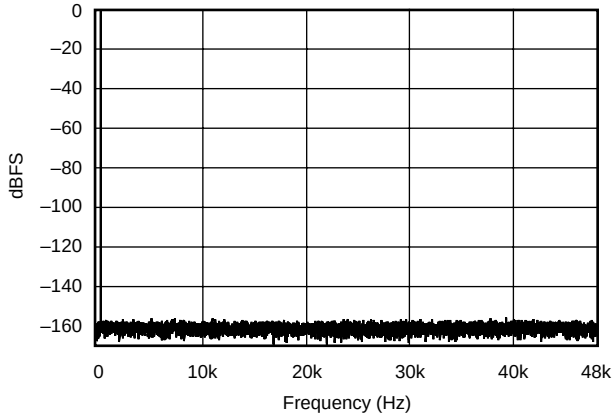
FFT with 1kHz INPUT TONE at –60dBFS
(48kHz:44.1kHz)



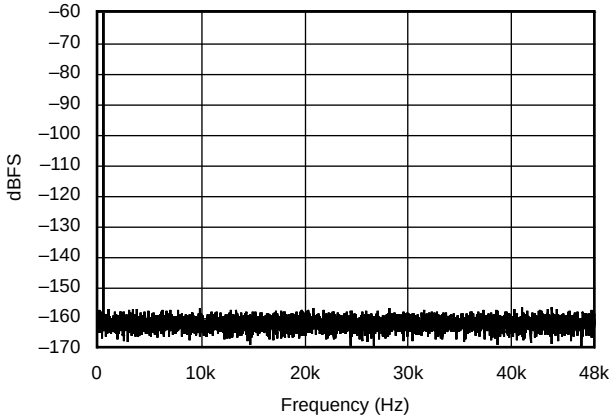
TYPICAL CHARACTERISTICS (Cont.)

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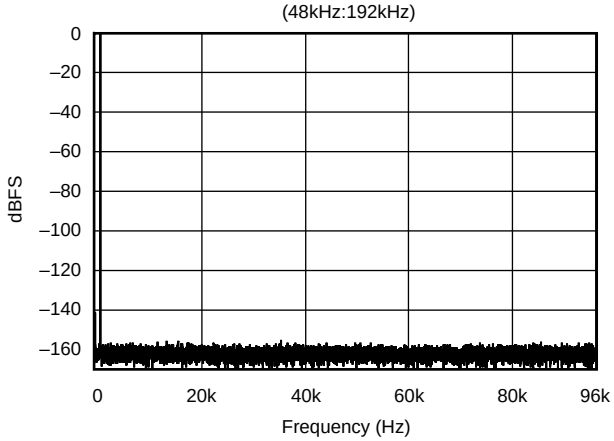
FFT with 1kHz INPUT TONE at 0dBFS
(48kHz:96kHz)



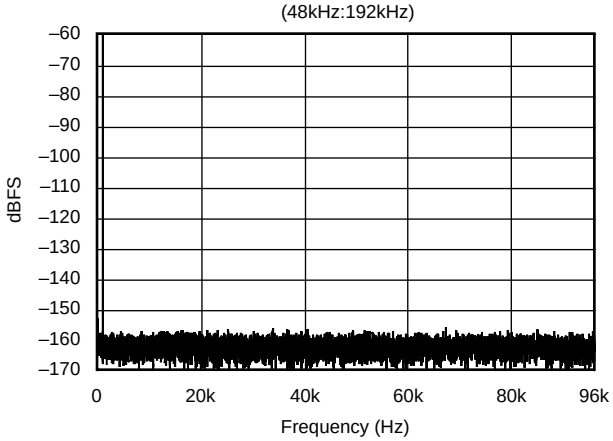
FFT with 1kHz INPUT TONE at –60dBFS
(48kHz:96kHz)



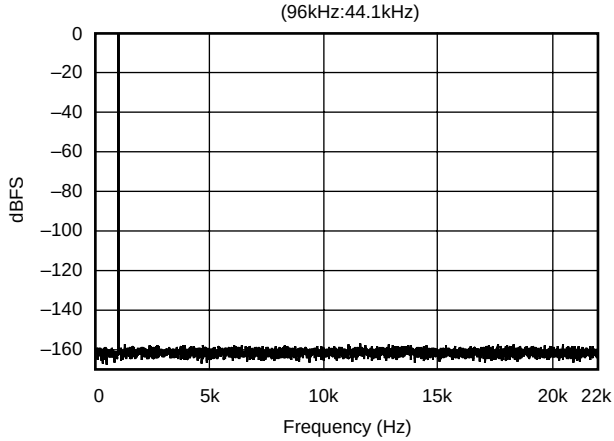
FFT with 1kHz INPUT TONE at 0dBFS
(48kHz:192kHz)



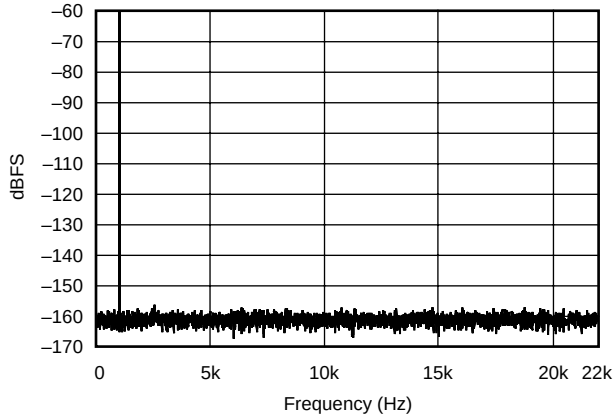
FFT with 1kHz INPUT TONE at –60dBFS
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FFT with 1kHz INPUT TONE at 0dBFS
(96kHz:44.1kHz)



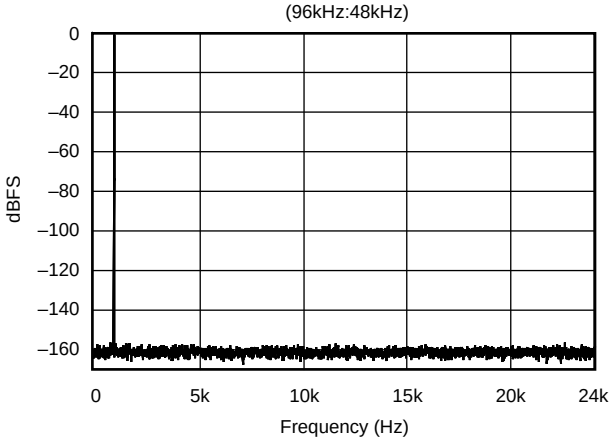
FFT with 1kHz INPUT TONE at –60dBFS
(96kHz:44.1kHz)



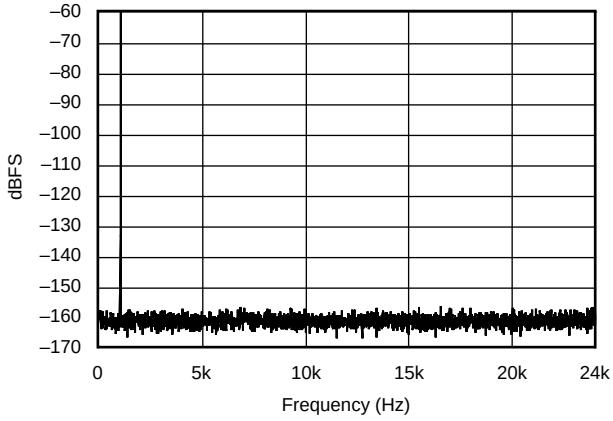
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_{DD} = +3.3V, and V_{IO} = +3.3V, unless otherwise noted.

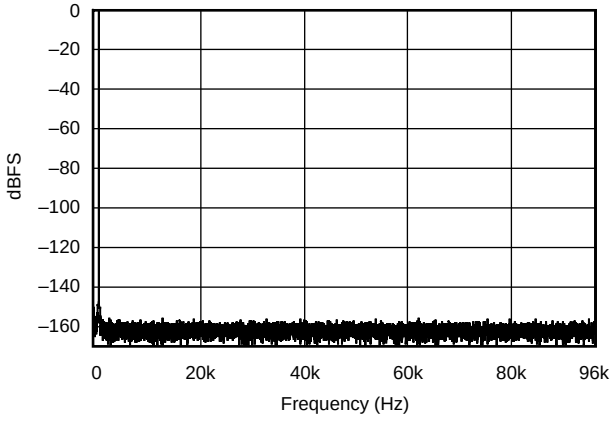
FFT with 1kHz INPUT TONE at 0dBFS
(96kHz:48kHz)



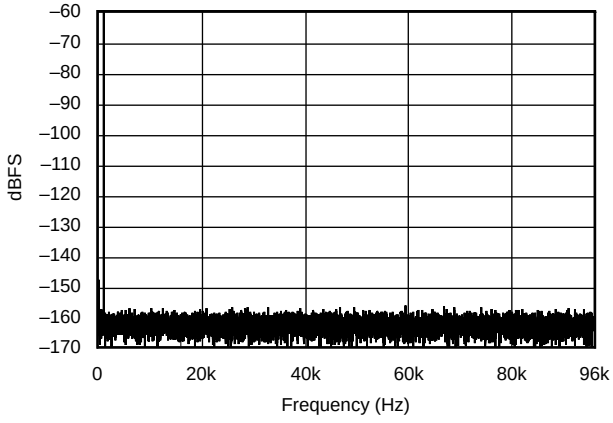
FFT with 1kHz INPUT TONE at –60dBFS
(96kHz:48kHz)



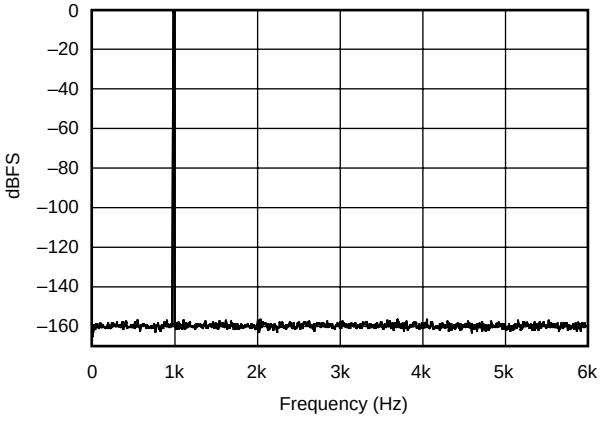
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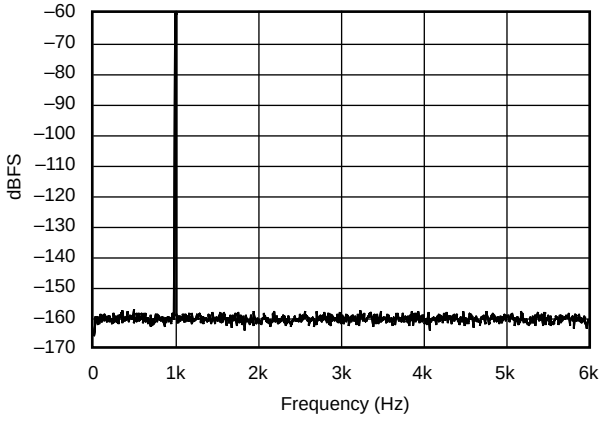
FFT with 1kHz INPUT TONE at –60dBFS
(96kHz:192kHz)



FFT with 1kHz INPUT TONE at 0dBFS
(192kHz:12kHz)



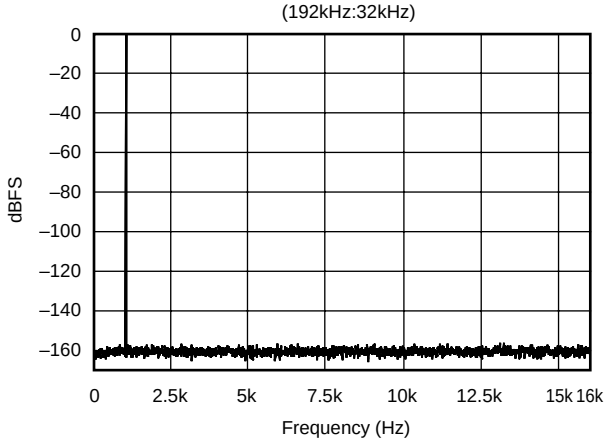
FFT with 1kHz INPUT TONE at –60dBFS
(192kHz:12kHz)



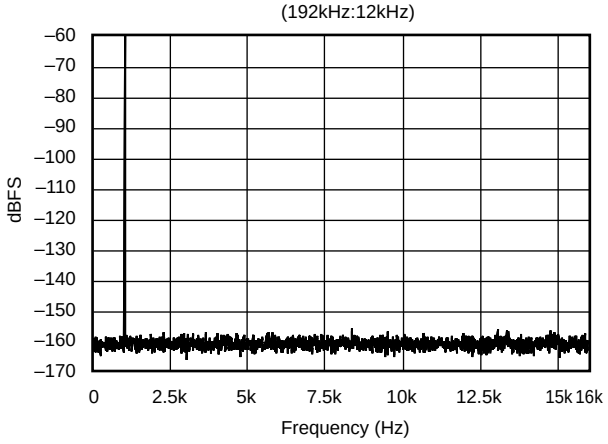
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_{DD} = +3.3V, and V_{IO} = +3.3V, unless otherwise noted.

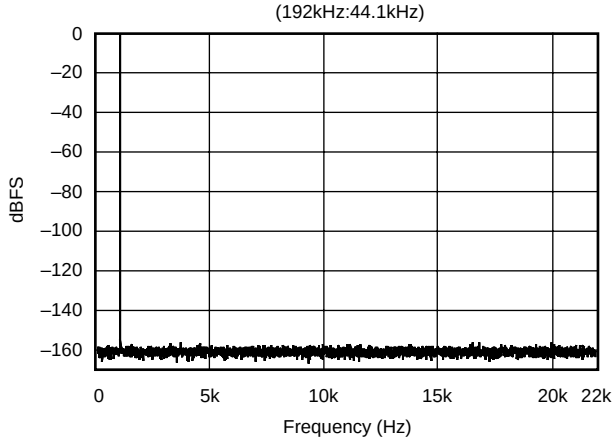
FFT with 1kHz INPUT TONE at 0dBFS
(192kHz:32kHz)



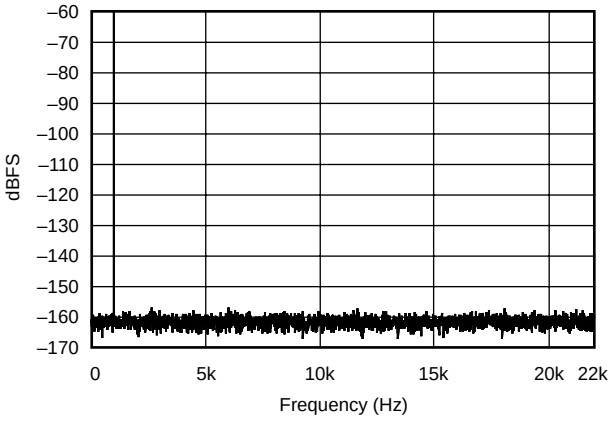
FFT with 1kHz INPUT TONE at –60dBFS
(192kHz:12kHz)



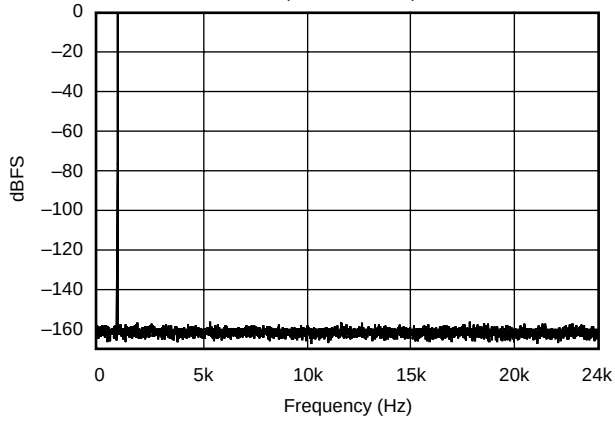
FFT with 1kHz INPUT TONE at 0dBFS
(192kHz:44.1kHz)



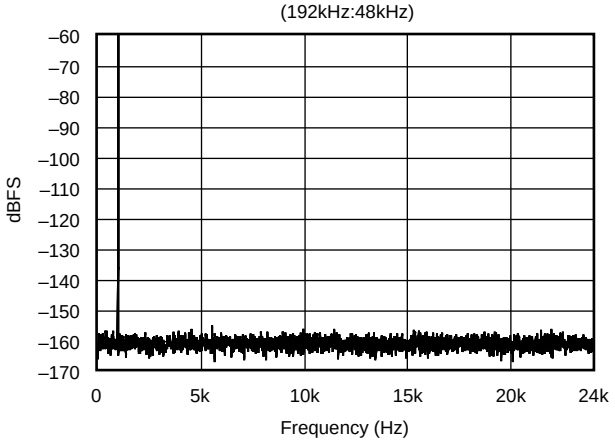
FFT with 1kHz INPUT TONE at –60dBFS
(192kHz:44.1kHz)



FFT with 1kHz INPUT TONE at 0dBFS
(192kHz:48kHz)



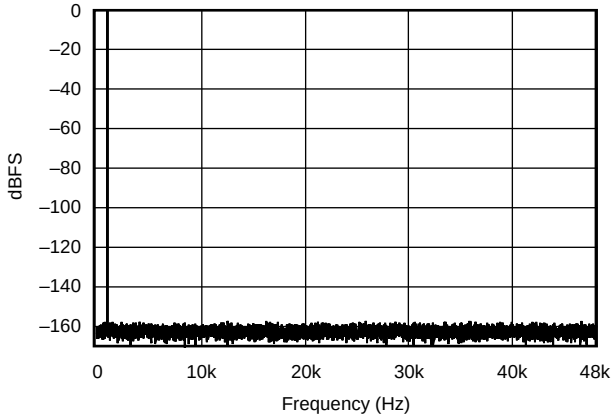
FFT with 1kHz INPUT TONE at –60dBFS
(192kHz:48kHz)



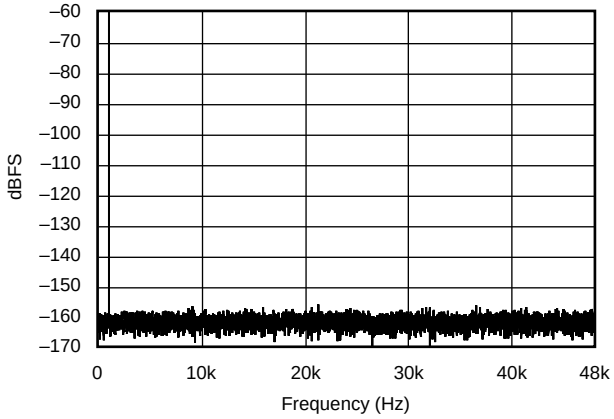
TYPICAL CHARACTERISTICS (Cont.)

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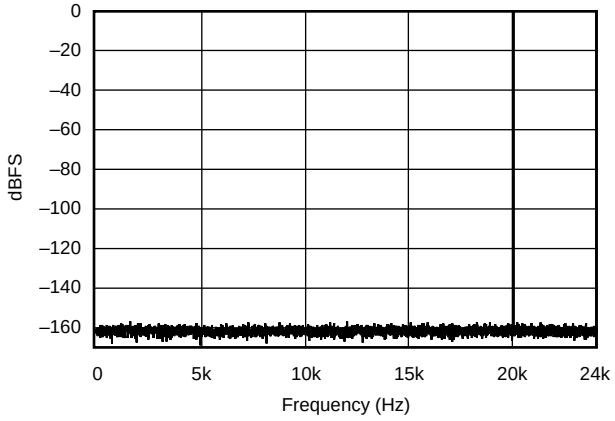
FFT with 1kHz INPUT TONE at 0dBFS
(192kHz:96kHz)



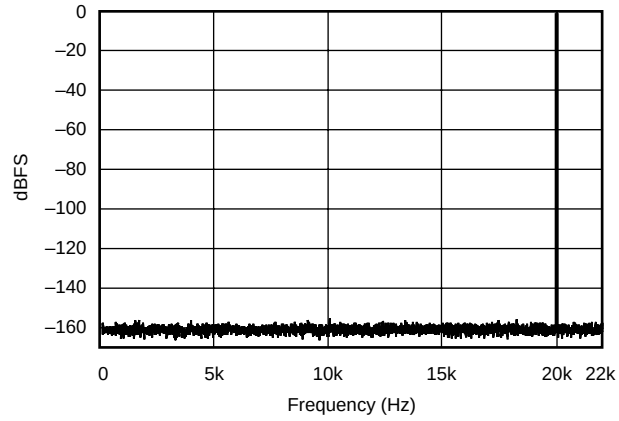
FFT with 1kHz INPUT TONE at –60dBFS
(192kHz:96kHz)



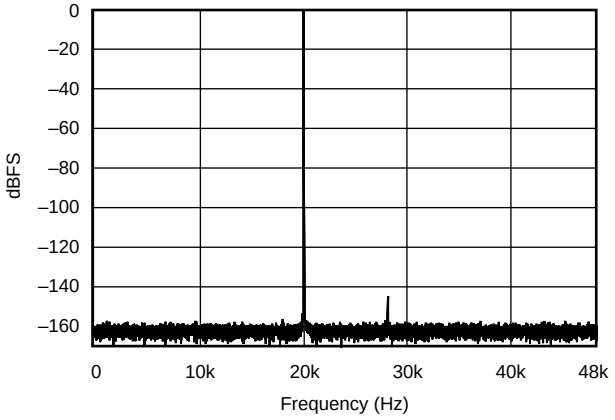
FFT with 20kHz INPUT TONE at 0dBFS
(44.1kHz:48kHz)



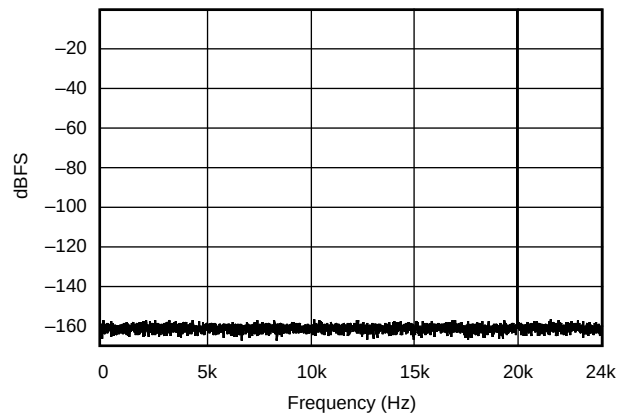
FFT with 20kHz INPUT TONE at 0dBFS
(48kHz:44.1kHz)



FFT with 20kHz INPUT TONE at 0dBFS
(48kHz:96kHz)



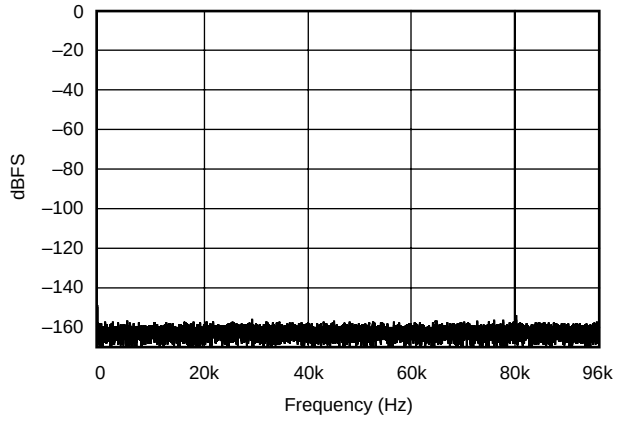
FFT with 20kHz INPUT TONE at 0dBFS
(96kHz:48kHz)



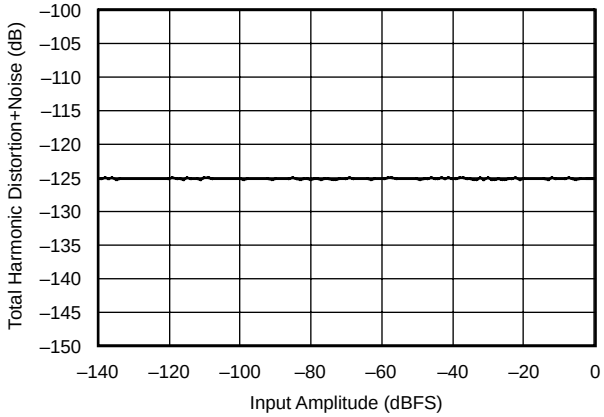
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_{DD} = +3.3V, and V_{IO} = +3.3V, unless otherwise noted.

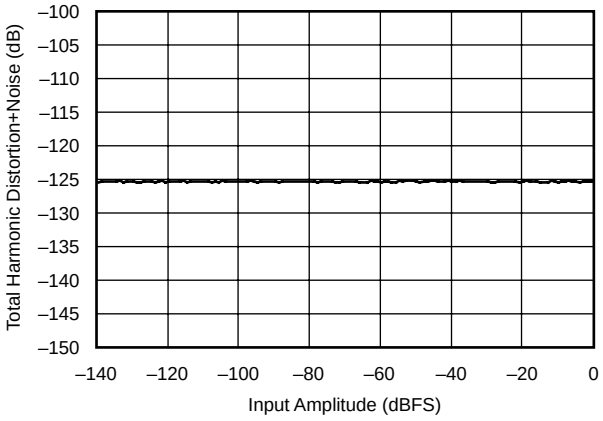
FFT with 80kHz INPUT TONE at 0dBFS
(192kHz:192kHz)



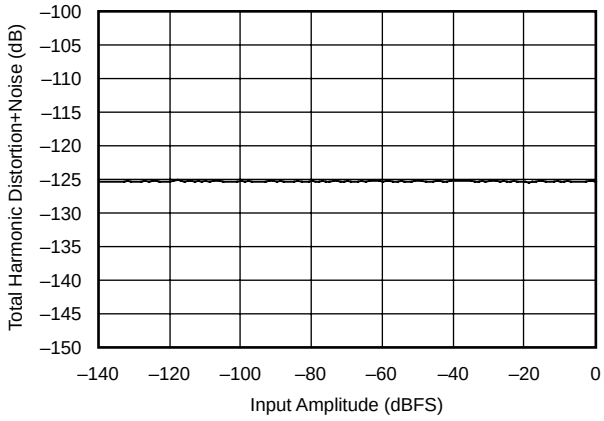
THD+N vs INPUT AMPLITUDE f_{IN} = 1kHz
(44.1kHz:48kHz)



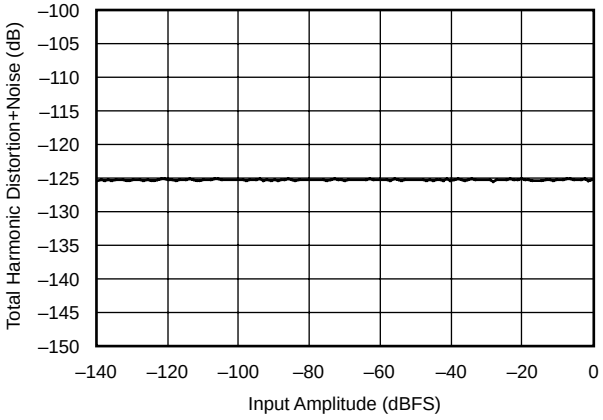
THD+N vs INPUT AMPLITUDE f_{IN} = 1kHz
(48kHz:44.1kHz)



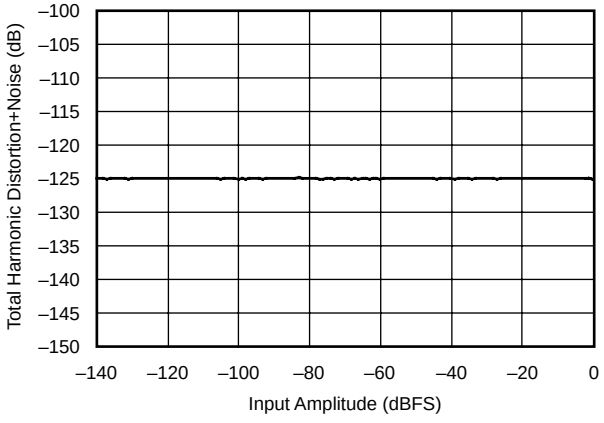
THD+N vs INPUT AMPLITUDE f_{IN} = 1kHz
(48kHz:96kHz)



THD+N vs INPUT AMPLITUDE f_{IN} = 1kHz
(96kHz:48kHz)



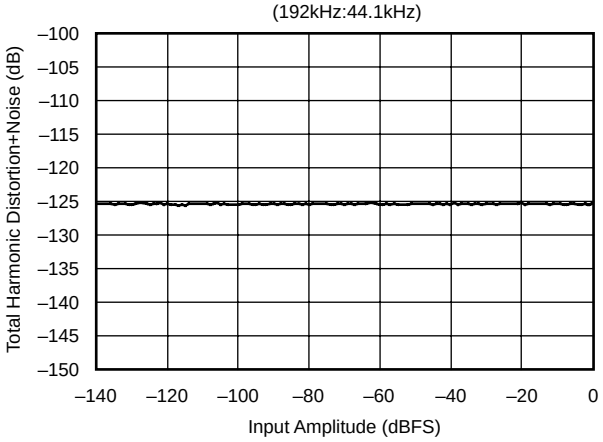
THD+N vs INPUT AMPLITUDE f_{IN} = 1kHz
(44.1kHz:192kHz)



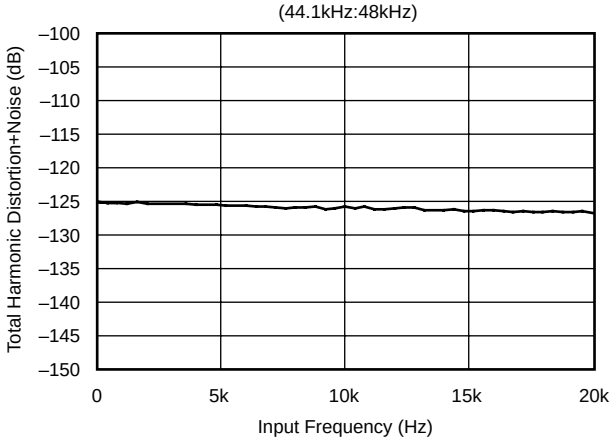
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_{DD} = +3.3V, and V_{IO} = +3.3V, unless otherwise noted.

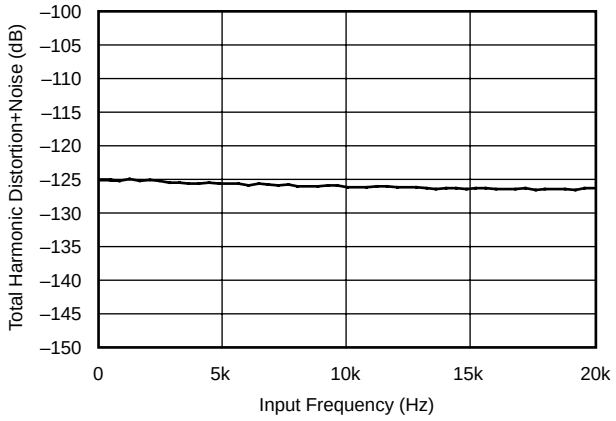
THD+N vs INPUT AMPLITUDE f_{IN} = 1kHz
(192kHz:44.1kHz)



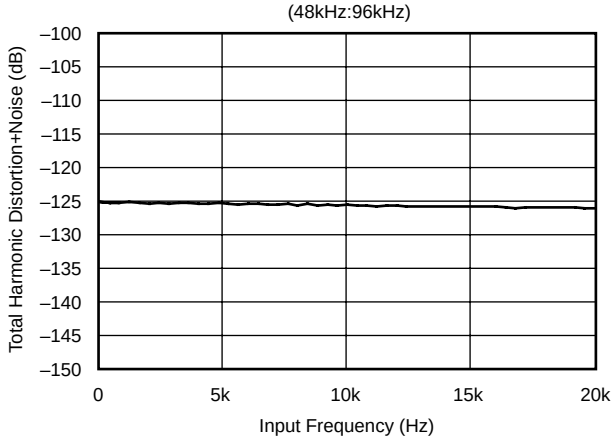
THD+N vs INPUT FREQUENCY WITH 0dBFS INPUT
(44.1kHz:48kHz)



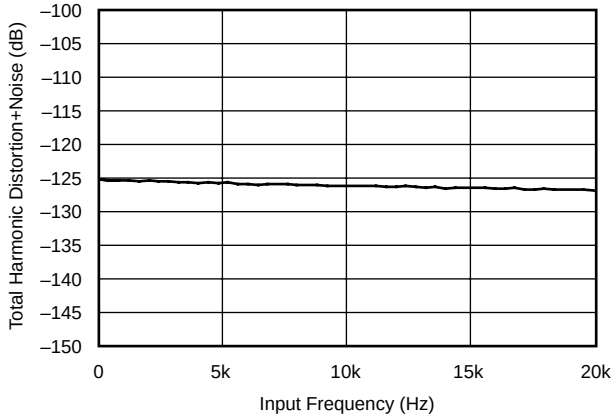
THD+N vs INPUT FREQUENCY WITH 0dBFS INPUT = 1kHz
(48kHz:44.1kHz)



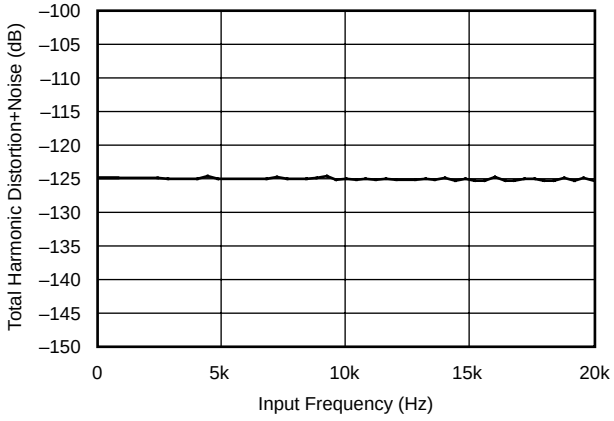
THD+N vs INPUT FREQUENCY WITH 0dBFS
(48kHz:96kHz)



THD+N vs INPUT FREQUENCY WITH 0dBFS
(96kHz:48kHz)



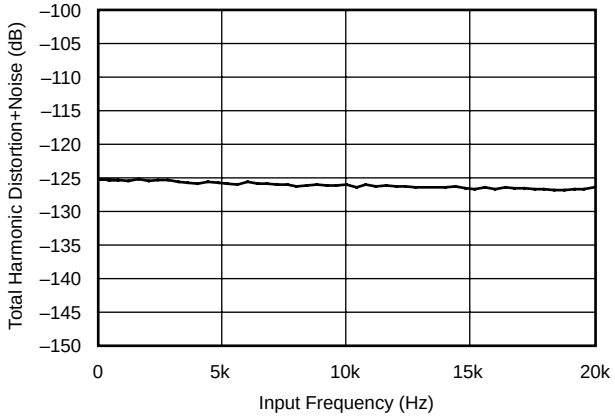
THD+N vs INPUT FREQUENCY WITH 0dBFS
(44.1kHz:192kHz)



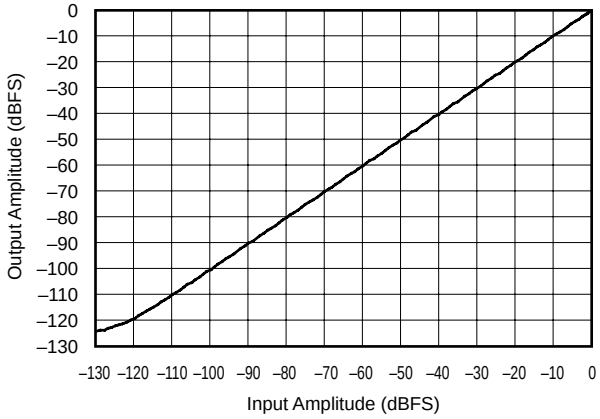
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_{DD} = +3.3V, and V_{IO} = +3.3V, unless otherwise noted.

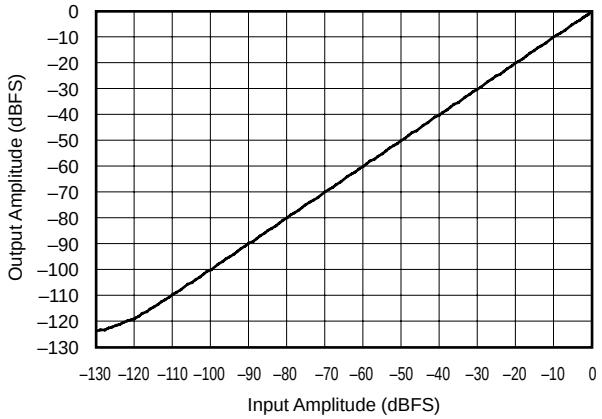
THD+N vs INPUT FREQUENCY WITH 0dBFS
(192kHz:44.1kHz)



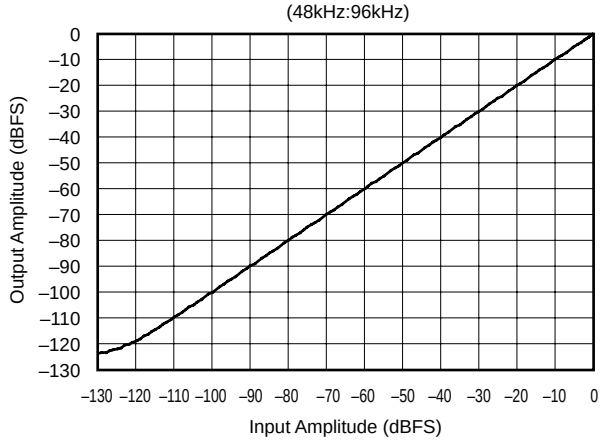
LINEARITY with f_{IN} = 200Hz
(44.1kHz:48kHz)



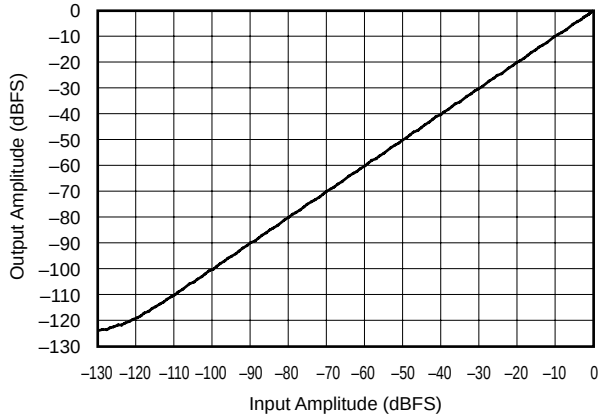
LINEARITY with f_{IN} = 200Hz
(48kHz:44.1kHz)



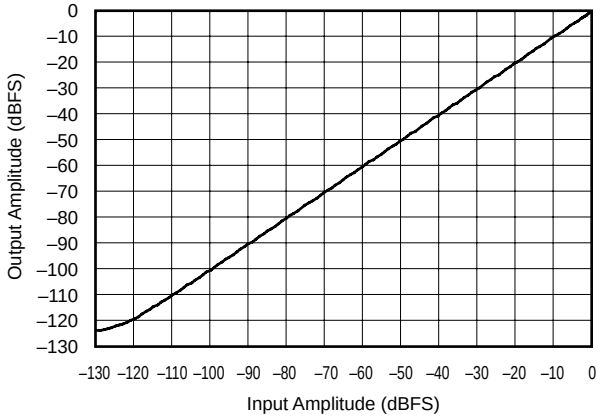
LINEARITY with f_{IN} = 200Hz
(48kHz:96kHz)



LINEARITY with f_{IN} = 200Hz
(96kHz:48kHz)



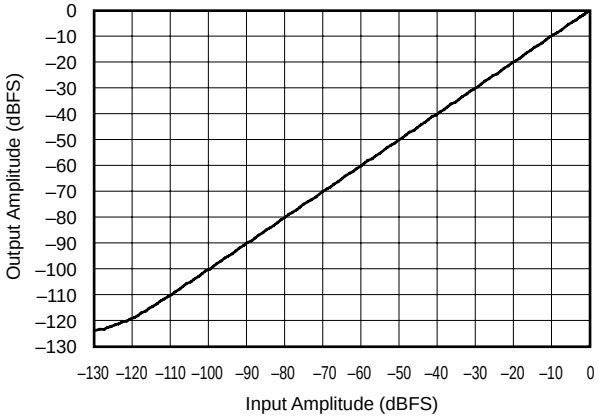
LINEARITY with f_{IN} = 200Hz
(44.1kHz:192kHz)



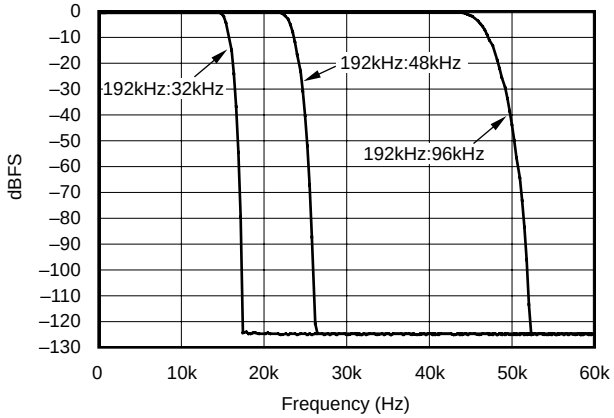
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_{DD} = +3.3V, and V_{IO} = +3.3V, unless otherwise noted.

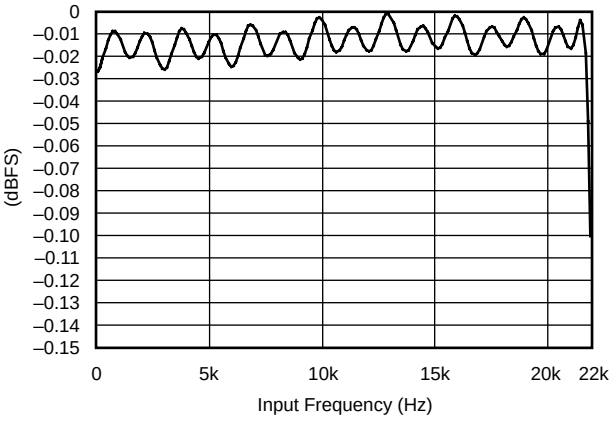
LINEARITY with f_{IN} = 200Hz
(192kHz:44.1kHz)



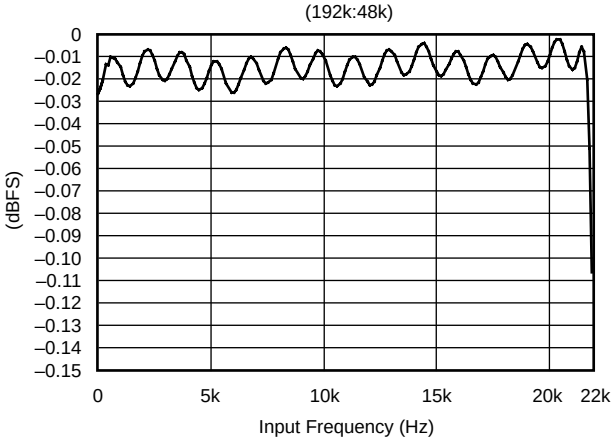
FREQUENCY RESPONSE with 0dBFS INPUT



PASS BAND RIPPLE
(48k:48k)



PASS BAND RIPPLE
(192k:48k)



PRODUCT OVERVIEW

The SRC4190 is an asynchronous sample rate converter (ASRC) designed for professional audio applications. Operation at input and output sampling frequencies up to 212kHz is supported, with an input/output sampling ratio range of 16:1 to 1:16. Excellent dynamic range and Total Harmonic Distortion + Noise (THD+N) are achieved by employing high performance and linear phase digital filtering. Digital filtering options allow for lower group delay processing.

The audio input and output ports support standard audio data formats, as well as a TDM interface mode. Word lengths of 24-, 20-, 18-, and 16-bits are supported. Both ports may operate in Slave mode, deriving their word and bit clocks from external input and output devices. Alternatively, one port may operate in Master mode while the other remains in Slave mode. In Master mode, the LRCK and BCK clocks are derived from the reference clock input, RCKI. The flexible configuration of the input and output ports allows connection to a wide variety of audio data converters, interface devices, digital signal processors, and programmable logic.

A bypass mode is included, which allows audio data to be passed directly from the input port to the output port, bypassing the ASRC function. The bypass option is useful for passing through encoded or compressed audio data, or non-audio control or status data.

A soft mute function is available providing artifact-free operation while muting the audio output signal. The mute attenuation is typically –128dB.

FUNCTIONAL BLOCK DIAGRAM

Figure 1 shows a functional block diagram of the SRC4190. Audio data is received at the input port, clocked by either the audio data source in Slave mode or by the SRC4190 in Master mode. The output port data is clocked by either the audio data source in Slave mode, or by the SRC4190 in Master mode. The input data is passed through interpolation filters which up-sample the data, which is then passed on to the re-sampler. The rate estimator compares the input and output sampling frequencies by comparing LRCKI, LRCKO, and a reference clock. The results include an offset for the FIFO pointer and the coefficients needed for re-sampling function.

The output of the re-sampler is then passed on to the decimation filter. The decimation filter performs down-sampling and anti-alias filtering functions.

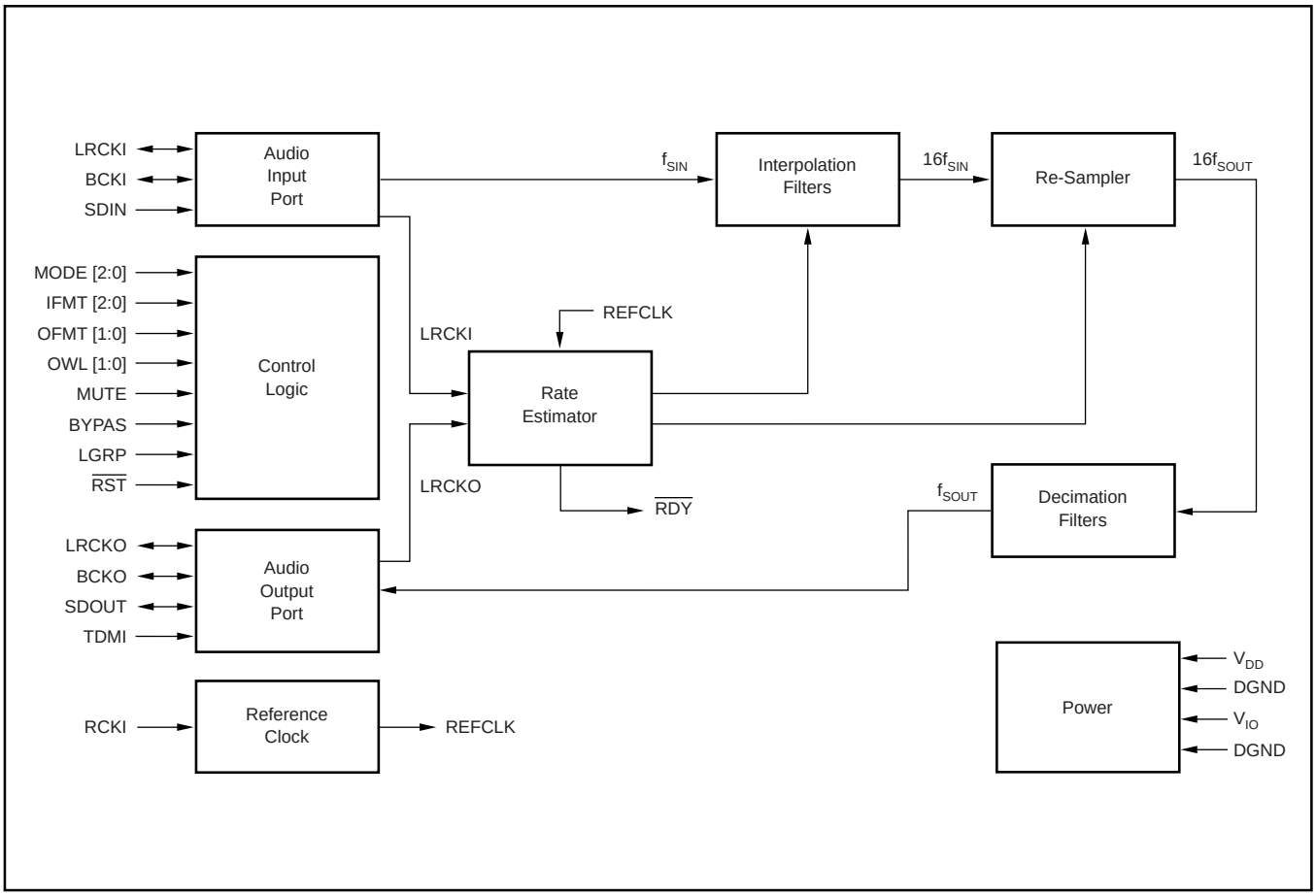


FIGURE 1. SRC4190 Functional Block Diagram.

REFERENCE CLOCK

The SRC4190 requires a reference clock for operation. The reference clock is applied at the RCKI input, pin 2. Figure 2 illustrates the reference clock connections and requirements for the SRC4190. The reference clock may operate at $128f_S$, $256f_S$, or $512f_S$, where f_S is the input or output sampling frequency. The maximum external reference clock input frequency is 50 MHz.

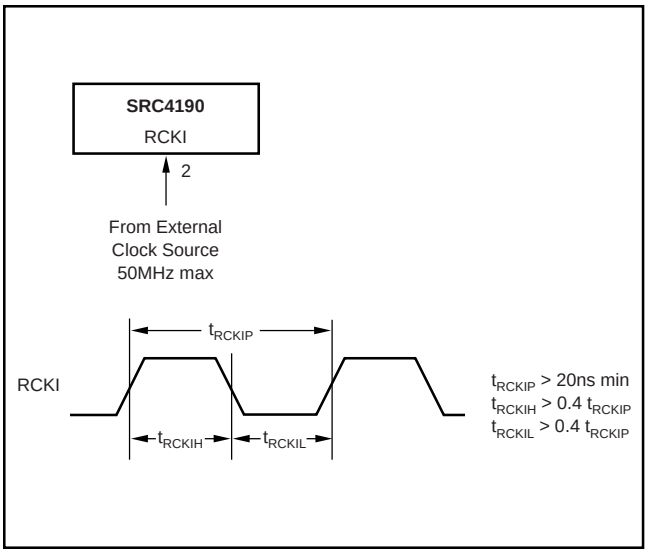


FIGURE 2. Reference Clock Input Connections and Timing Requirements.

RESET AND POWER DOWN OPERATION

The SRC4190 may be reset using the $\overline{RST}$ input (pin 13). There is no internal power on reset, so the user should force a reset sequence after power up in order to initialize the device. In order to force a reset, the reference clock input must be active, with an external clock source supplying a valid reference clock signal (refer to Figure 2). The user must assert $\overline{RST}$ low for a minimum of 500 nanoseconds and then bring $\overline{RST}$ high again to force a reset. Figure 3 shows the reset timing for the SRC4190.

The SRC4190 also supports a power-down mode. Power-down mode may be set by holding the $\overline{RST}$ input low.

AUDIO PORT MODES

The SRC4190 supports seven serial port modes, which are shown in Table 1. The audio port mode is selected using the MODE0 (pin 26), MODE1 (pin 27), and MODE2 (pin 28) inputs.

In Slave mode, the port LRCK and BCK clocks are configured as inputs, and receive their clocks from an external audio device. In Master mode, the LRCK and BCK clocks are configured as outputs, being derived from the reference clock input (RCKI). Only one port can be set to Master mode at any given time, as indicated in Table 1.

MODE2	MODE1	MODE0	SERIAL PORT MODE
0	0	0	Both Input and Output Ports are Slave mode
0	0	1	Output Port is Master mode with RCKI = $128f_S$
0	1	0	Output Port is Master mode with RCKI = $512f_S$
0	1	1	Output Port is Master mode with RCKI = $256f_S$
1	0	0	Both Input and Output Ports are Slave Mode
1	0	1	Input Port is Master mode with RCKI = $128f_S$
1	1	0	Input Port is Master mode with RCKI = $512f_S$
1	1	1	Input Port is Master mode with RCKI = $256f_S$

TABLE 1. Setting the Serial Port Modes.

INPUT PORT OPERATION

The audio input port is a three-wire synchronous serial interface that may operate in either Slave or Master mode. The SDIN input (pin 4) is the serial audio data input. Audio data is input at this pin in one of three standard audio data formats: Philips I^2S, Left Justified, or Right Justified. The audio data word length may be up to 24 bits for I^2S and Left Justified formats, while the Right Justified format supports 16-, 18-, 20-, or 24-bit data. The data formats are shown in Figure 4, while critical timing parameters are shown in Figure 5 and listed in the Electrical Characteristics table.

The bit clock is either an input or output at BCKI (pin 5). In slave mode, BCKI is configured as an input pin, and may operate at rates from $32f_S$ to $128f_S$, with a minimum of one clock cycle per data bit. In Master mode, BCKI operates at a fixed rate of $64f_S$.

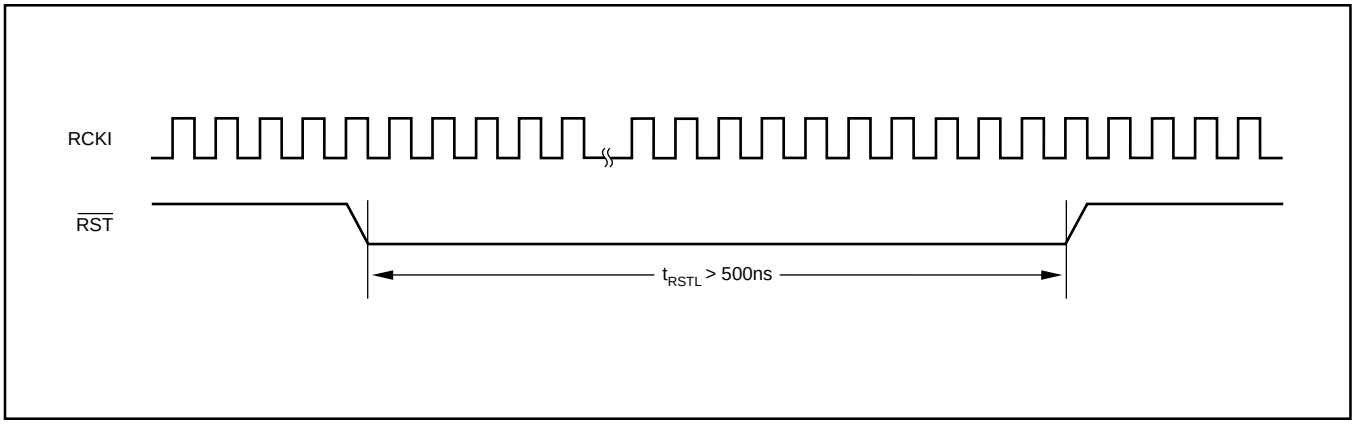


FIGURE 3. Reset Pulse Width Requirement.

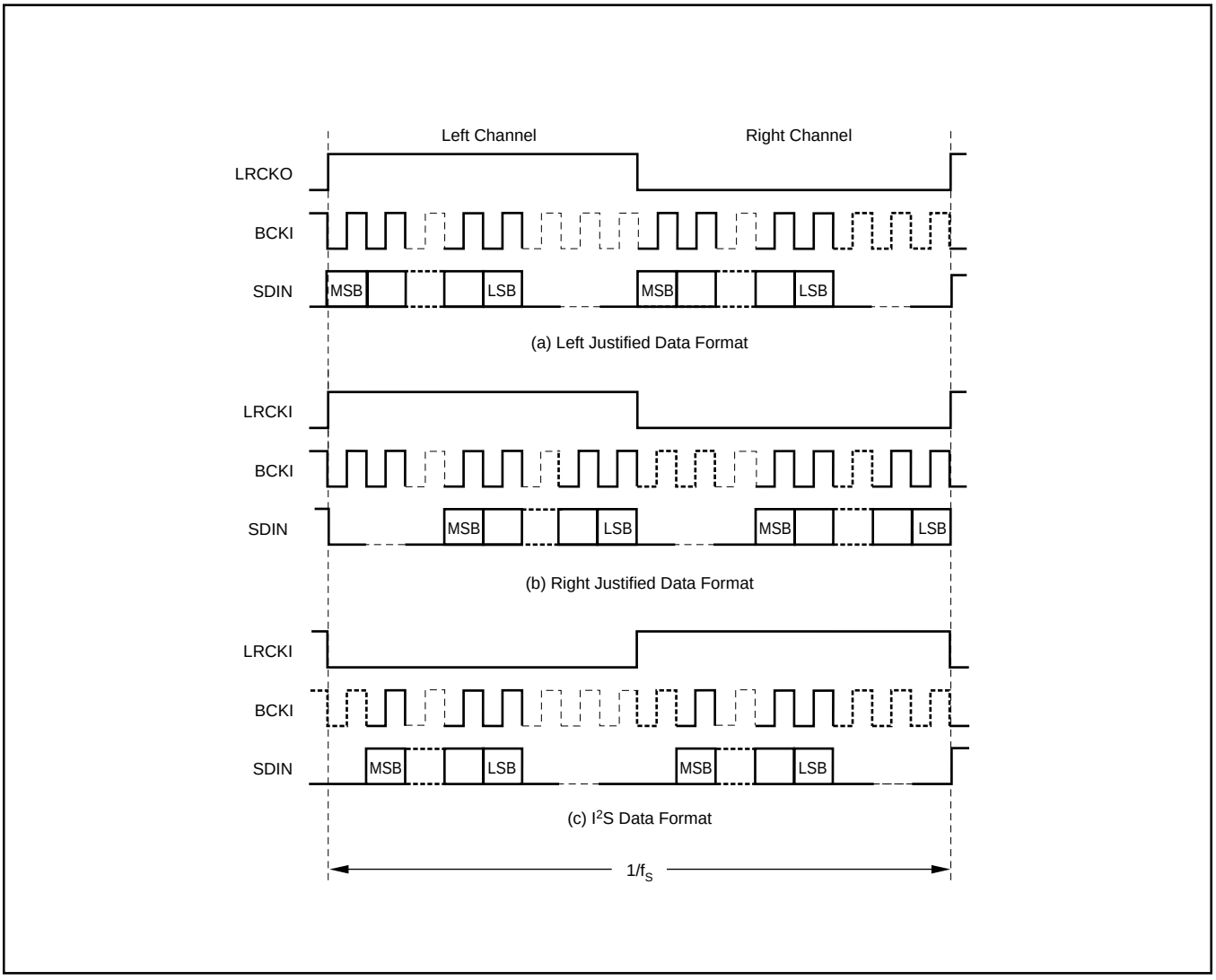


FIGURE 4. Input Data Formats.

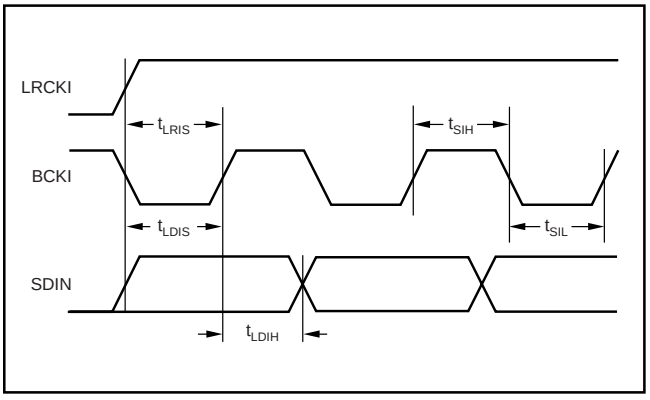


FIGURE 5. Input Port Timing.

The left/right word clock, LRCKI (pin 6), may be configured as an input or output pin. In Slave mode, LRCKI is an input pin, while in Master mode LRCKI is an output pin. In either case, the clock rate is equal to f_S, the input sampling frequency. The LRCKI duty cycle is fixed to 50% for Master mode operation.

Table 2 illustrates data format selection for the input port. The IFMT0 (pin 10), IFMT1 (pin 11), and IFMT2 (pin 12) inputs are utilized to set the input port data format.

IFMT2	IFMT1	IFMT0	INPUT PORT DATA FORMAT
0	0	0	24-Bit Left Justified
0	0	1	24-Bit I²S
0	1	0	Unused
0	1	1	Unused
1	0	0	16-Bit Right Justified
1	0	1	18-Bit Right Justified
1	1	0	20-Bit Right Justified
1	1	1	24-Bit Right Justified

TABLE 2. Input Port Data Format Selection.

OUTPUT PORT OPERATION

The audio output port is a four-wire synchronous serial interface that may operate in either Slave or Master mode. The SDOUT output (pin 23) is the serial audio data output. Audio data is output at this pin in one of four data formats: Philips I²S, Left Justified, Right Justified, or TDM. The audio data word length may be 16-, 18-, 20-, or 24-bits. For all word lengths, the data is triangular PDF dithered from the internal 28-bit data path. The data formats (with the exception of TDM mode) are shown in Figure 6, while critical timing parameters are shown in Figure 7 and listed in the Electrical Characteristics table. The TDM format and timing are shown in Figures 11 and 12, respectively, while examples of standard TDM configurations are shown in Figures 13 and 14.

The bit clock is either input or output at BCKO (pin 25). In Slave mode, BCKO is configured as an input pin, and may operate at rates from $32f_S$ to $128f_S$, with a minimum of one clock cycle for each data bit. The exception is the TDM mode, where the BCKO must operate at N x $64f_S$, where N is equal to the number of SRC4190 devices included on the TDM interface. In Master mode, BCKO operates at a fixed rate of $64f_S$ for all data formats except TDM, where BCKO operates at the reference clock (RCKI) frequency. Additional information regarding TDM mode operation is included in the Applications Information section of this data sheet.

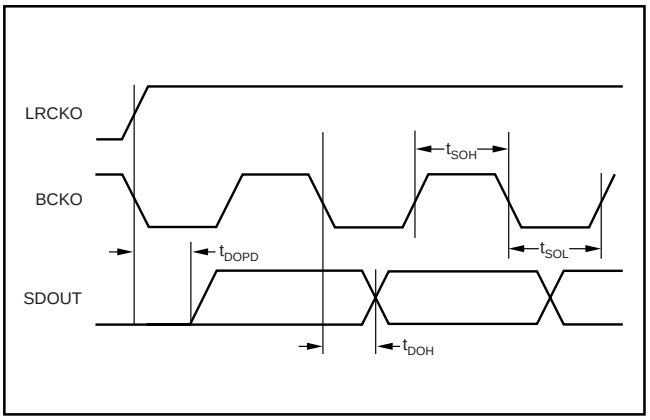


FIGURE 7. Output Port Timing.

The left/right word clock, LRCKO (pin 24), may be configured as an input or output pin. In Slave mode, LRCKO is an input pin, while in Master mode it is an output pin. In either case, the clock rate is equal to f_S, the output sampling frequency. The clock duty cycle is fixed to 50% for I²S, Left Justified, and Right Justified formats in Master mode. The LRCKO pulse width is fixed to 32 BCKO cycles for the TDM format in Master mode.

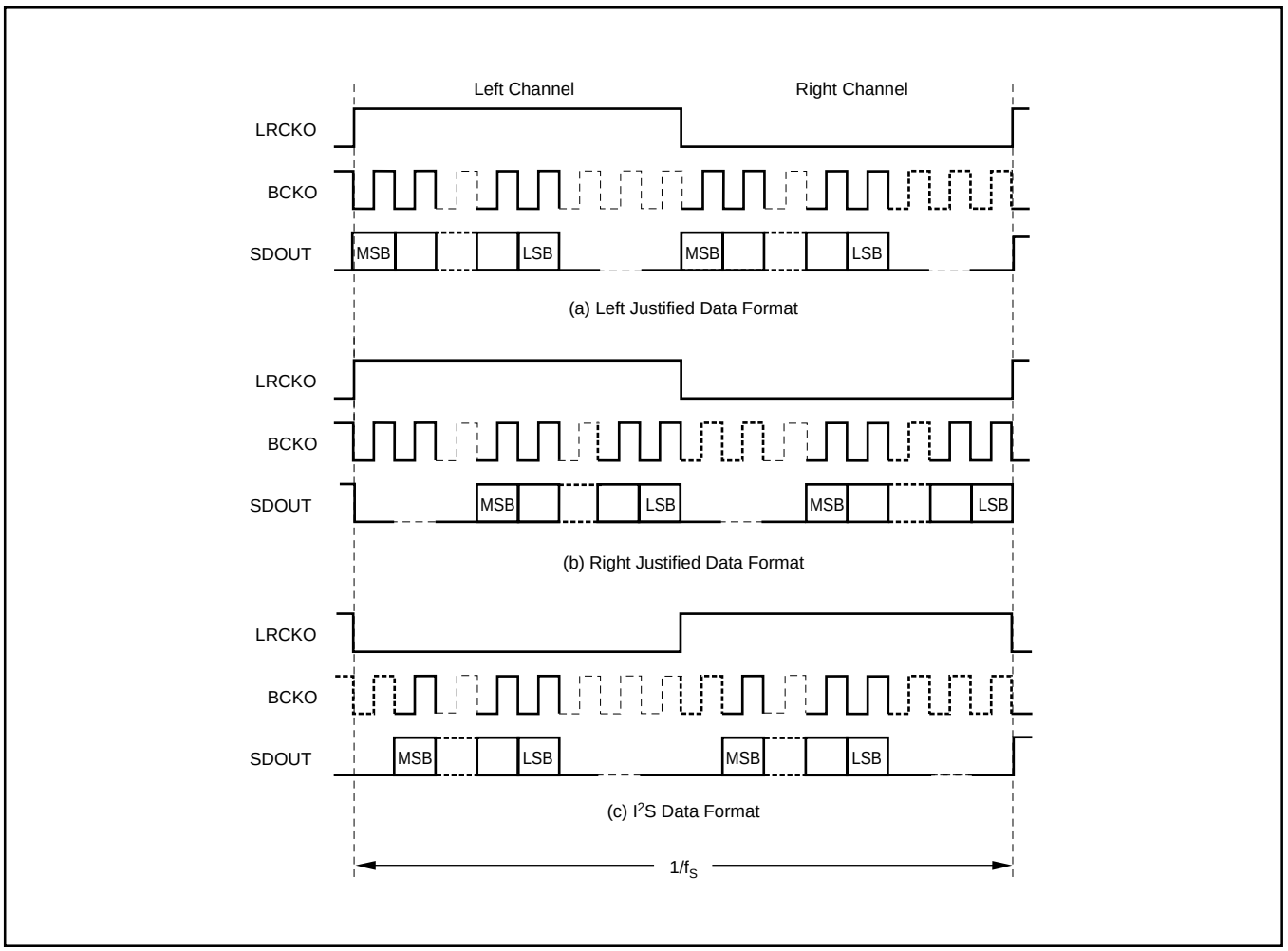


FIGURE 6. Output Data Formats.

Table 3 illustrates data format selection for the output port. The OFMT0 (pin 19), OFMT1 (pin 18), OWL0 (pin 17), and OWL1 (pin 16) inputs are utilized to set the output port data format and word length.

OFMT1	OFMT0	OUTPUT PORT DATA FORMAT
0	0	Left Justified
0	1	I^2S
1	0	TDM
1	1	Right Justified
OWL1	**OWL0**	**OUTPUT PORT DATA WORD LENGTH**
0	0	24 Bits
0	1	20 Bits
1	0	18 Bits
1	1	16 Bits

TABLE 3. Output Port Data Format Selection.

BYPASS MODE

The SRC4190 includes a bypass function, which routes the input port data directly to the output port, bypassing the ASRC function. Bypass mode may be invoked by forcing the BYPAS input (pin 9) high. For normal ASRC operation, the BYPAS pin should be set to 0.

No dithering is applied to the output data in bypass mode; digital attenuation and mute functions are also unavailable in this mode.

SOFT MUTE FUNCTION

The soft mute function of the SRC4190 may be invoked by forcing the MUTE input (pin 14) high. The Soft mute function slowly attenuates the output signal level down to all zeroes plus ±4LSB of dither. This provides an artifact-free muting of the audio output port.

READY OUTPUT

The SRC4190 includes an active low ready output named $\overline{RDY}$ (pin 15). This is an output from the rate estimator block, which indicates that the input-to-output sampling frequency ratio has been determined. The ready signal can be used as a flag or indicator output. The ready signal can also be connected to the active high MUTE input (pin 14) to provide an auto-mute function, so that the output port is muted when the rate estimator is in transition.

APPLICATIONS INFORMATION

This section of the data sheet provides practical applications information for hardware and systems engineers who will be designing the SRC4190 into their end equipment.

RECOMMENDED CIRCUIT CONFIGURATION

The typical connection diagram for the SRC4190 is shown in Figure 8. Recommended values for power supply bypass capacitors are included. These capacitors should be placed as close to the IC package as possible.

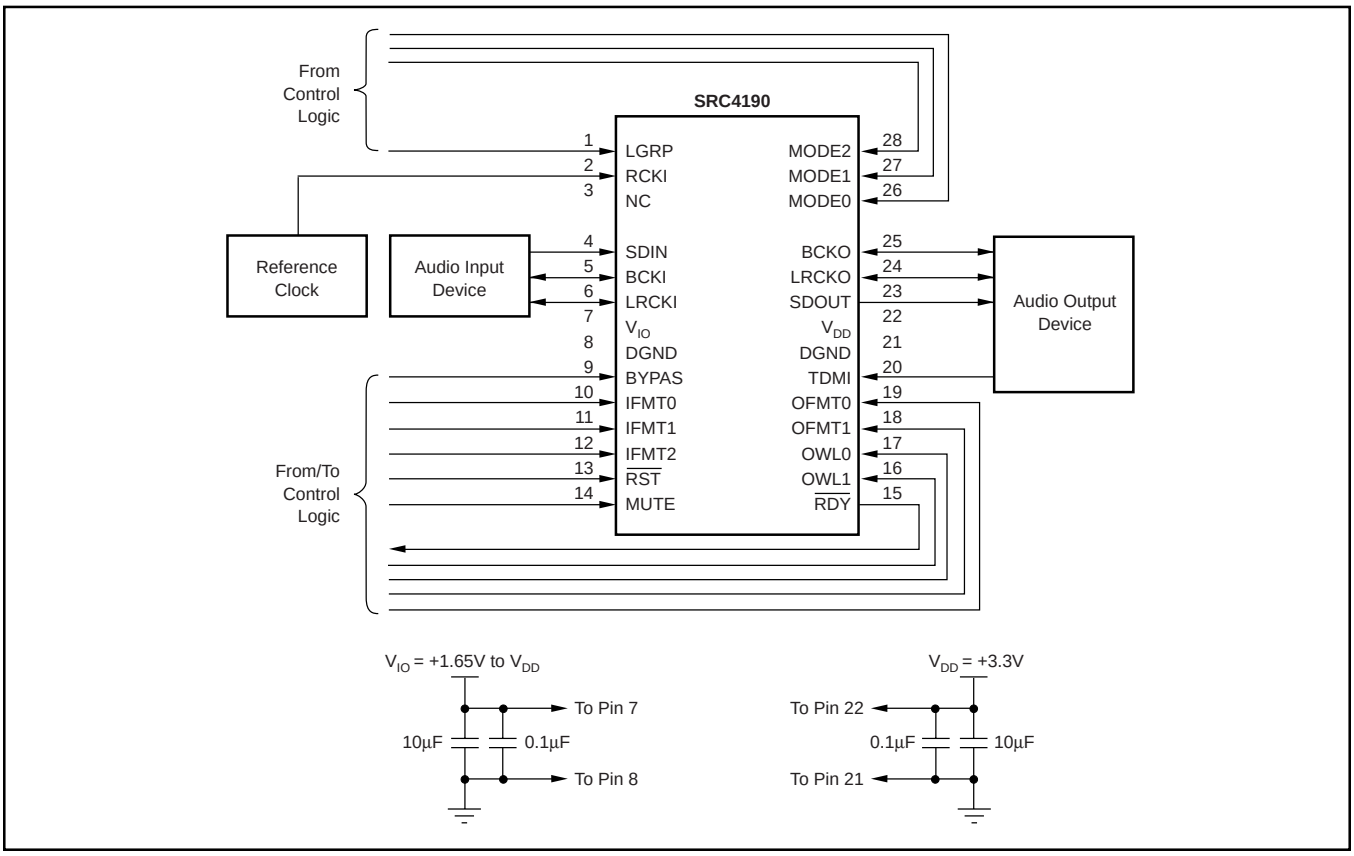


FIGURE 8. Typical Connection Diagram for the SRC4190.

INTERFACING TO DIGITAL AUDIO RECEIVERS AND TRANSMITTERS

The SRC4190 input and output ports are designed to interface to a variety of audio devices, including receivers and transmitters commonly used for AES/EBU, S/PDIF, and CP1201 communications.

Texas Instruments manufactures the DIR1703 digital audio interface receiver and DIT4096/4192 digital audio transmitters to address these applications.

Figure 9 illustrates interfacing the DIR1703 to the SRC4190 input port. The DIR1703 operates from a single +3.3V supply, which requires the V_{IO} supply (pin 7) for the SRC4190 to be set to +3.3V for interface compatibility.

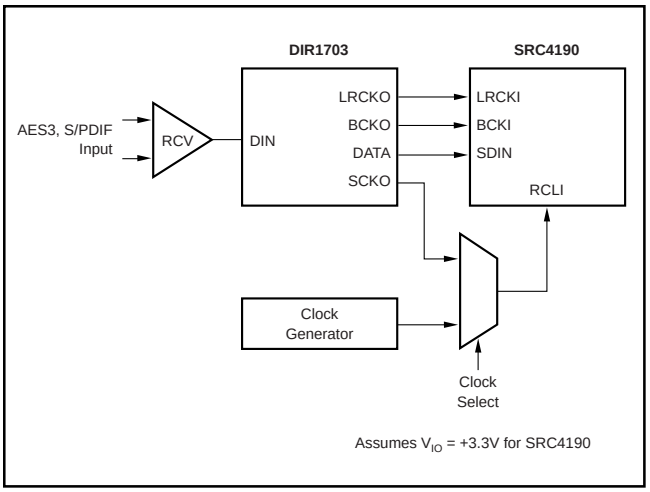


FIGURE 9. Interfacing the SRC4190 to the DIR1703 Digital Audio Interface Receiver.

Figure 10 shows the interface between the SRC4190 output port and the DIT4096 or DIT4192 audio serial port. Once again, the V_{IO} supplies for both the SRC4190 and DIT4096/4192 are set to +3.3V for compatibility.

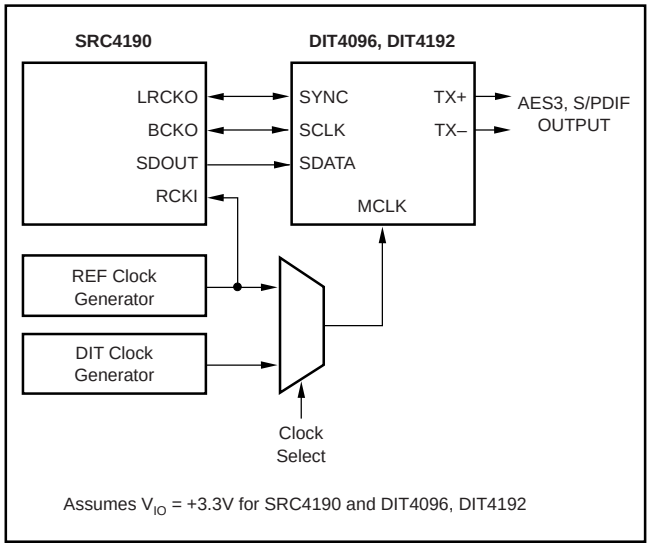


FIGURE 10. Interfacing the SRC4190 to the DIT4096/4192 Digital Audio Interface Transmitter.

Like the SRC4190 output port, the DIT4096 and DIT4192 audio serial port may be configured as a Master or Slave. In cases where the SRC4190 output port is set to Master mode, it is recommended to use the reference clock source (RCKI) as the master clock source (MCLK) for the DIT4096/4192, to ensure that the transmitter is synchronized to the SRC4190 output port data.

TDM APPLICATIONS

The SRC4190 supports a TDM output mode, which allows multiple devices to be daisy-chained together to create a serial frame. Each device occupies one sub-frame within a frame, and each sub-frame carries two channels (Left followed by Right). Each sub-frame is 64 bits long, with 32 bits allotted for each channel. The audio data for each channel is Left Justified within the allotted 32 bits. Figure 11 illustrates the TDM frame format, while Figure 12 shows the TDM input timing parameters, which are listed in the Electrical Characteristics table of this data sheet.

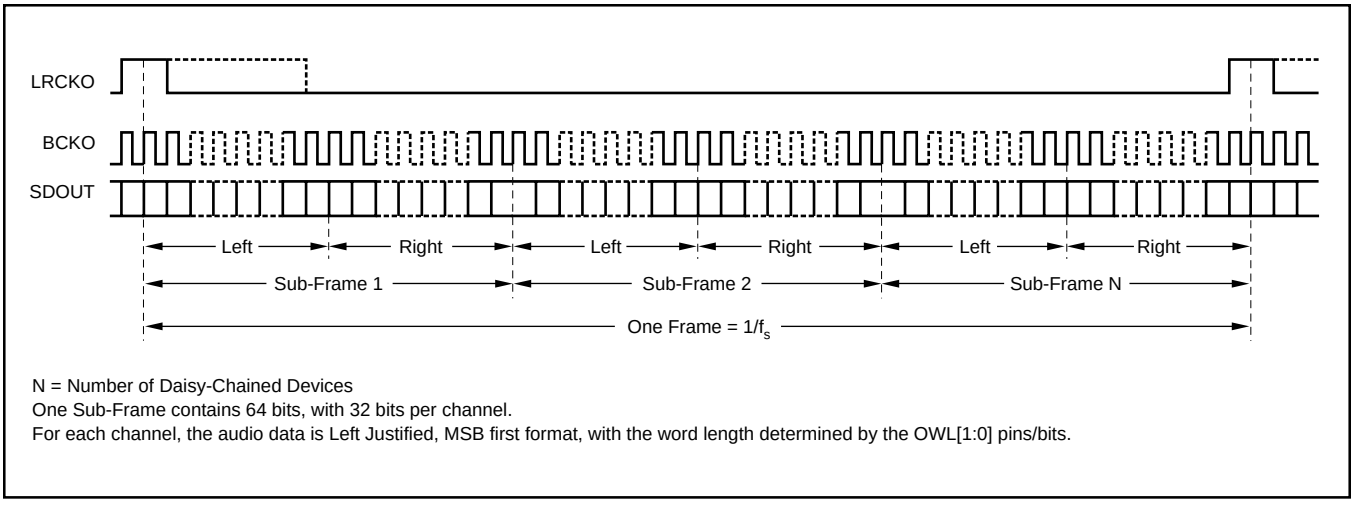


FIGURE 11. TDM Frame Format.

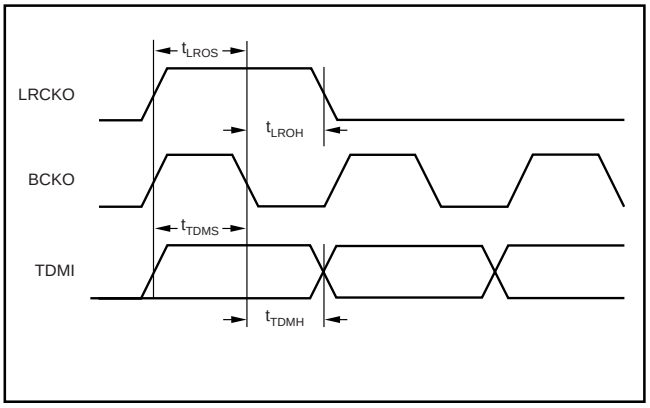


FIGURE 12. Input Timing for TDM Mode.

The frame rate is equal to the output sampling frequency, f_s. The BCKO frequency for the TDM interface is N x 64f_s, where N is the number of devices included in the daisy chain. For Master mode, the output BCKO frequency is fixed to the reference clock (RCKI) input frequency. The number of devices that can be daisy-chained in TDM mode is dependent upon the output sampling frequency and the BCKO frequency, leading to the following numerical relationship:

Number of Daisy-Chained Devices = (f_{BCKO} / f_s) / 64

Where:

f_{BCKO} = Output Port Bit Clock (BCKO), 27.136 MHz maximum

f_s = Output Port Sampling (or LRCKO) Frequency, 212kHz maximum.

This relationship holds true for both Slave and Master modes.

Figures 13 and 14 show typical connection schemes for the TDM mode. Although the TMS320C671x DSP family is shown as the audio processing engine in these figures, other TI digital signal processors with a multi-channel buffered serial port (McBSP™) may also function with this arrangement. Interfacing to processors from other manufacturers is also possible. Refer to Figure 7 in this data sheet, along with the equivalent serial port timing diagrams shown in the DSP data sheet, to determine compatibility.

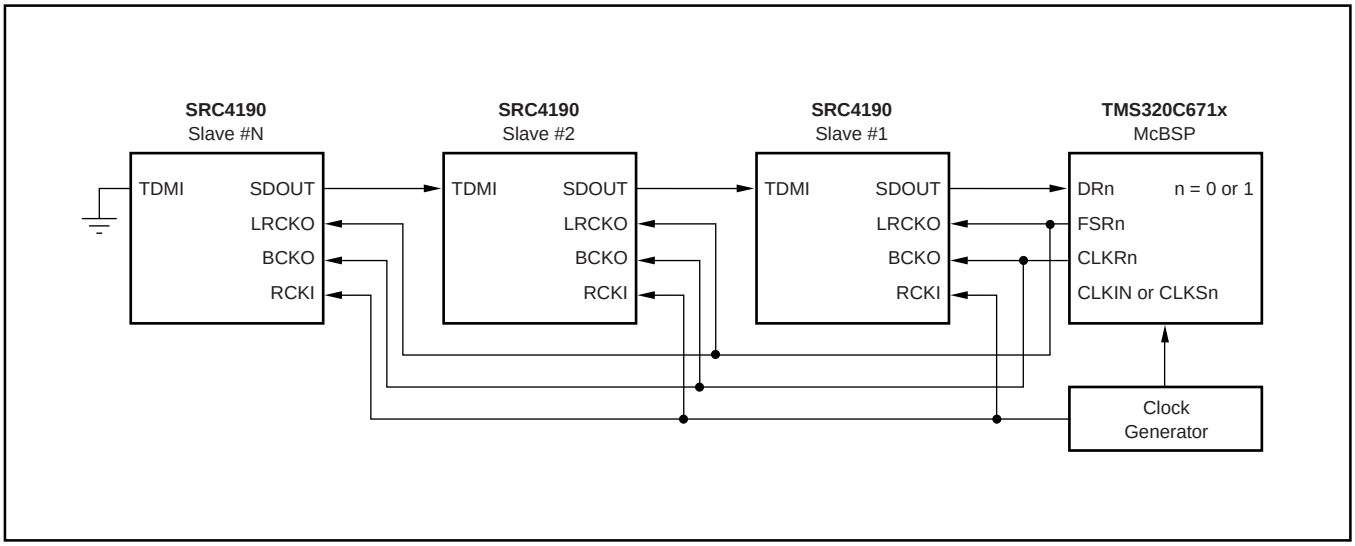


FIGURE 13. TDM Interface where all Devices are Slaves.

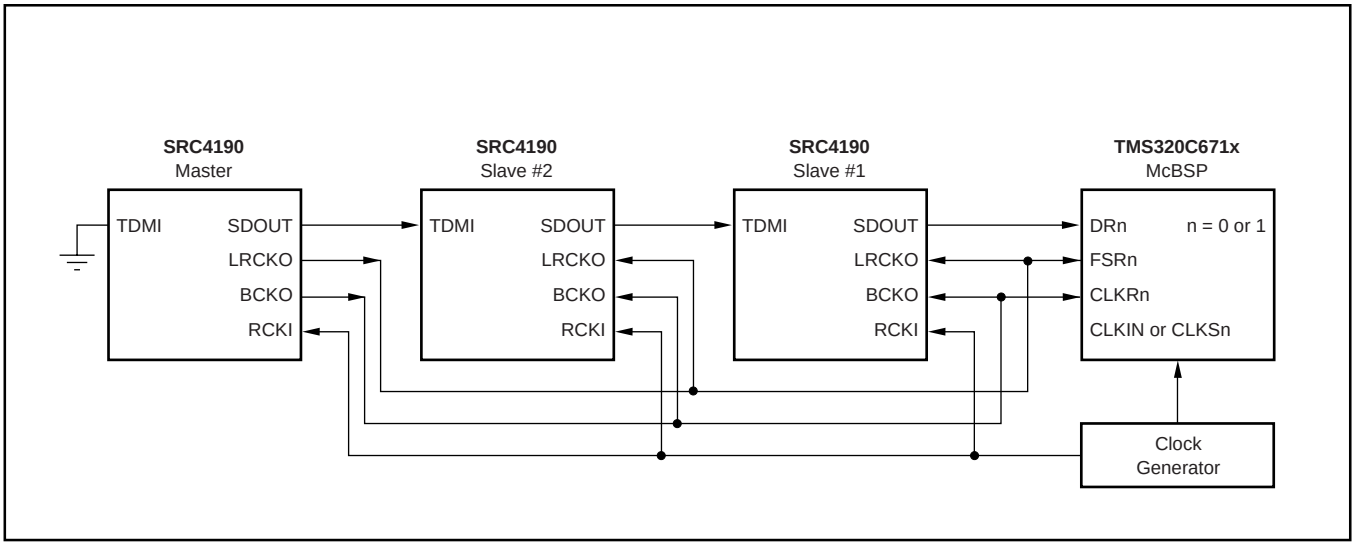


FIGURE 14. TDM Interface where one Device is Master to Multiple Slaves.

PIN COMPATIBILITY WITH THE ANALOG DEVICES AD1895 AND AD1896

The SRC4190 is pin-and function-compatible with the AD1895 and AD1896 when observing the guidelines indicated in the following paragraphs.

Power Supplies. To ensure compatibility, the VDD_IO and VDD_CORE supplies of the AD1895 and AD1896 must be set to +3.3V, while the V_{IO} and V_{DD} supplies of the SRC4190 must be set to +3.3V.

Pin 1 connection. For the AD1895, pin 1 is a no connect (N.C.) pin. For the SRC4190, pin 1 functions as the low group delay selection input, and should not be left unconnected. Pin 1 must be connected to either digital ground or the V_{IO} supply, dependent upon the desired group delay.

Crystal Oscillator. The SRC4190 does not have an on-chip crystal oscillator. An external reference clock is required at the RCKI input (pin 2).

Reference Clock Frequency. The reference clock input frequency for the SRC4190 must be no higher than 30 MHz, in order to match the master clock frequency specification of the AD1895 and AD1896. In addition, the SRC4190 does not support the $768f_S$ reference clock rate.

Master Mode Maximum Sampling Frequency. When the input or output ports are set to Master mode, the maximum sampling frequency must be limited to 96kHz in order to support the AD1895 and AD1896 specification. This is despite the fact that the SRC4190 supports a maximum sampling frequency of 212kHz in Master mode. The user should consider building an option into his or her design to support the higher sampling frequency of the SRC4190.

Matched Phase Mode. Due to the internal architecture of the SRC4190, it does not require or support the matched phase mode of the AD1896. Given multiple SRC4190 devices, if all reference clock (RCKI) inputs are driven from the same clock source, the devices will be phase matched.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SRC4190IDB	ACTIVE	SSOP	DB	28	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SRC4190IDBR	ACTIVE	SSOP	DB	28	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

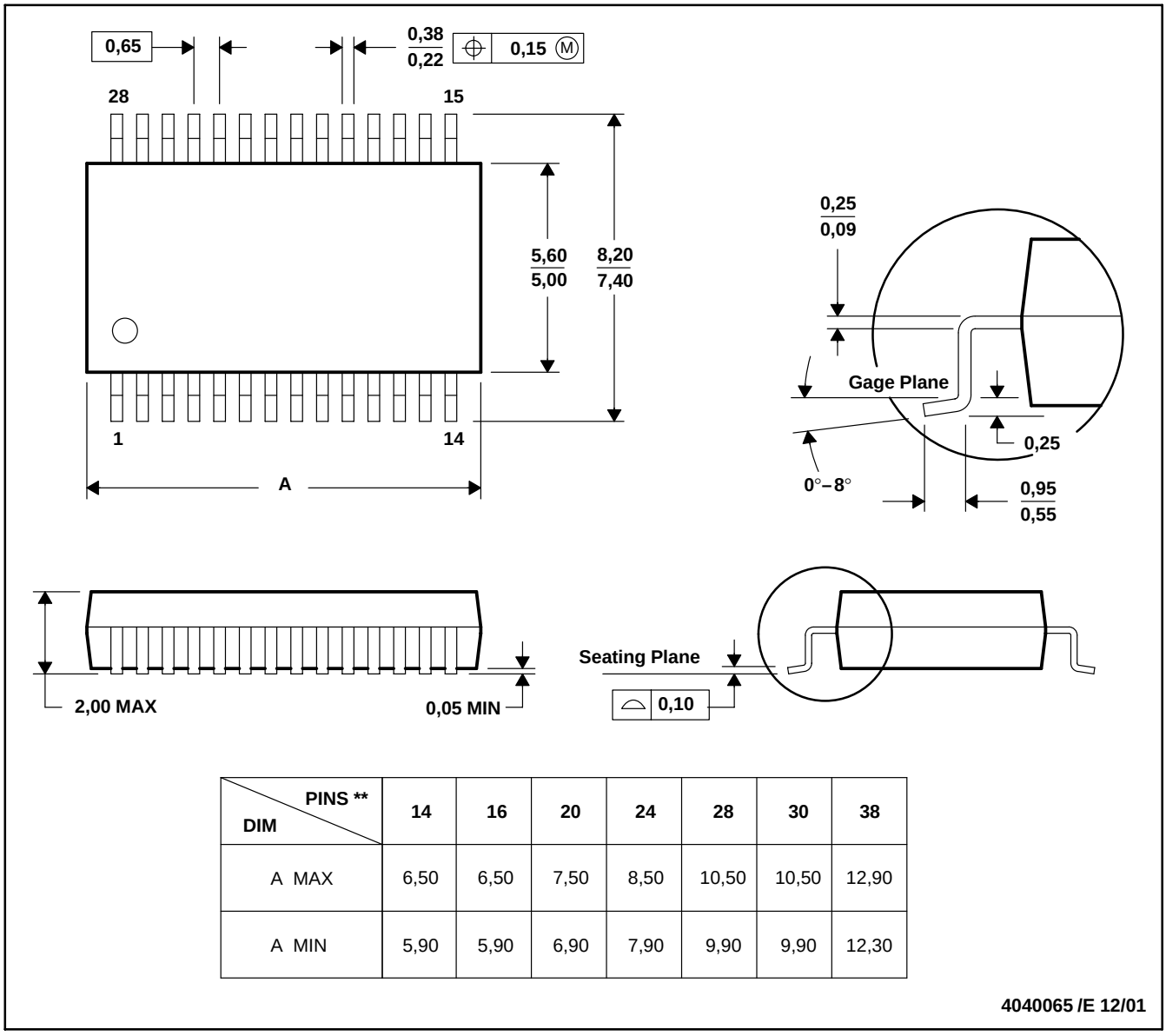
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DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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